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NOTES:  
1.HSF Property:Comply iSupplier system HSF property attribute up-to-date value.

A7

N18P-G62

2020.6.1

21OCT2002		
DATE	CHANGE NO.	REV

DESIGN/ DRAWER	XXX	DATE	21OCT2002
CHECK			
APPROVAL			
FILE TIME			
PCB P/N	0000000000	PCB VER	XXX

INVENTEC			
TITLE MODEL PROJECT FUNCTION			
MAIN BOARD			
SIZE A3	CODE GS	DOC NUMBER 13100000-00	REV 001
SHEET 1		of 10	

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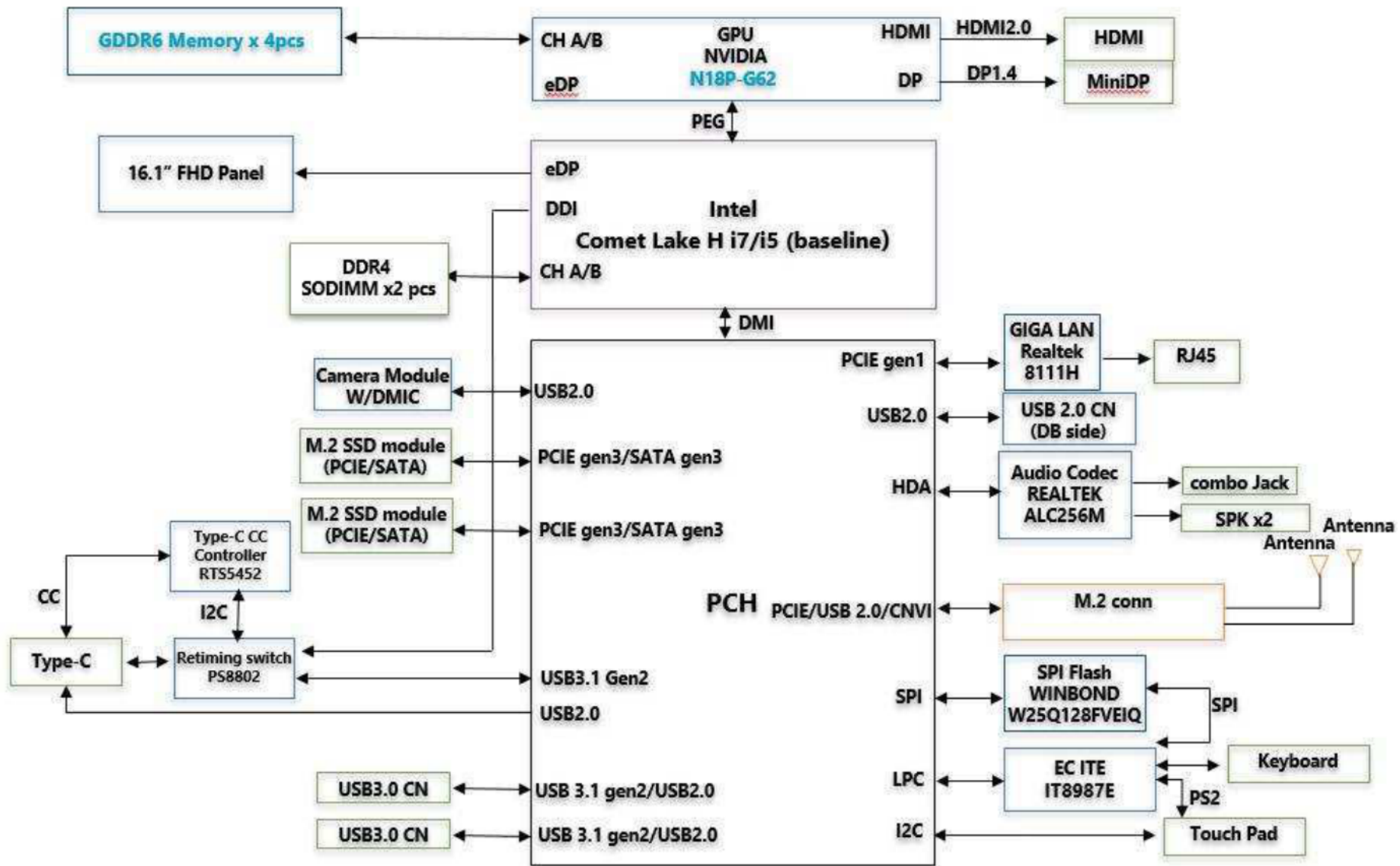
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INVENTEC

TITLE  
MODEL,PROJECT,FUNCTION  
TABLE OF THE CONTENT

CHANGE by PCB PIN	XXX 60xxxxxxxxxx	DATE PCB VER	21-OCT-2002 XXX	SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
SHEET				2	of	101	

# Block Diagram (N18P-G62)

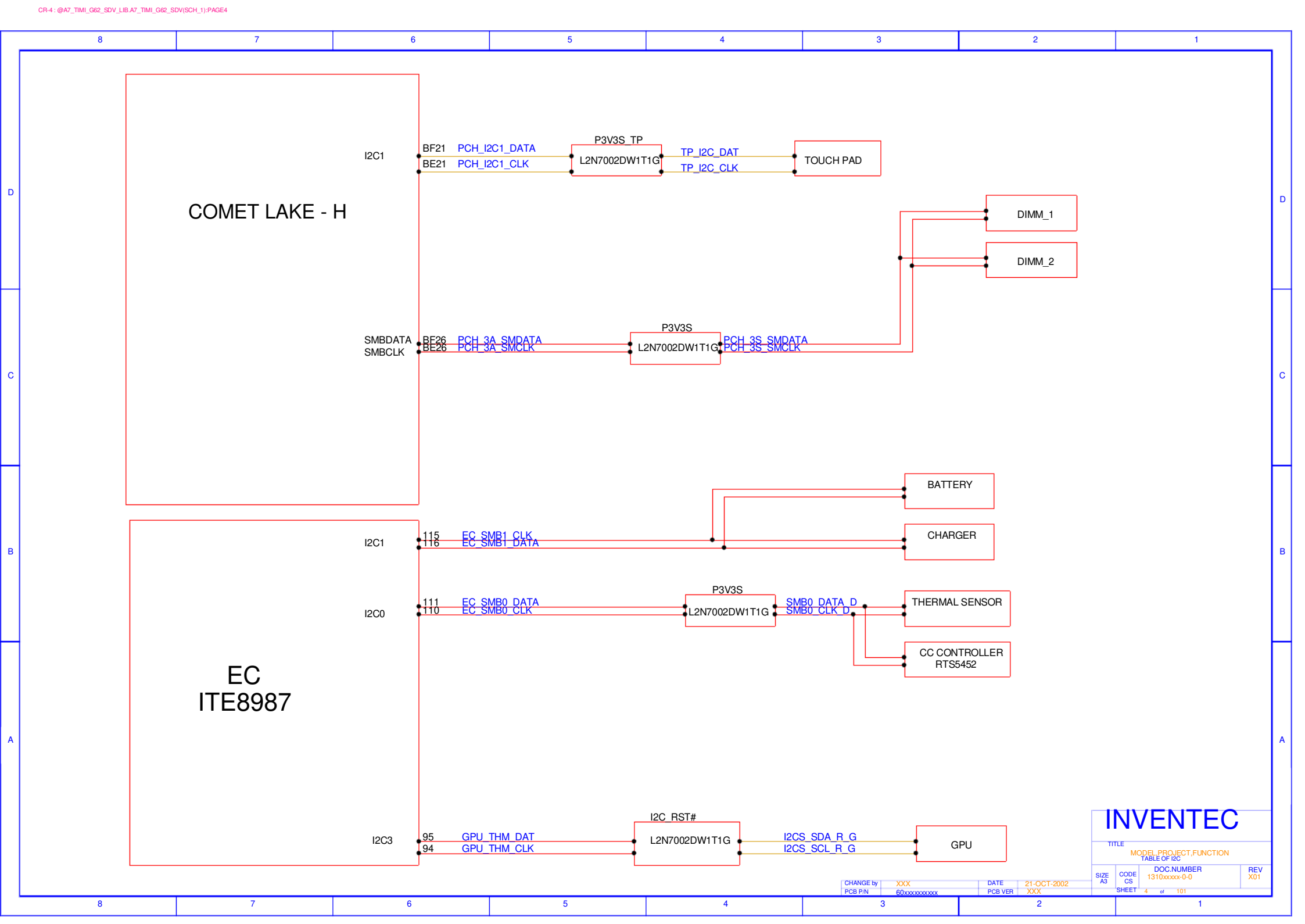
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MODEL PROJECT FUNCTION  
Block Diagram

SIZE CODE DOC NUMBER REV

A3 CS 1310xxxx-0-0 X01

SHEET 3 of 101

CHANGE by XXX  
PCB P/N 60xxxxxxx  
DATE 21-OCT-2002  
PCB VER XXX



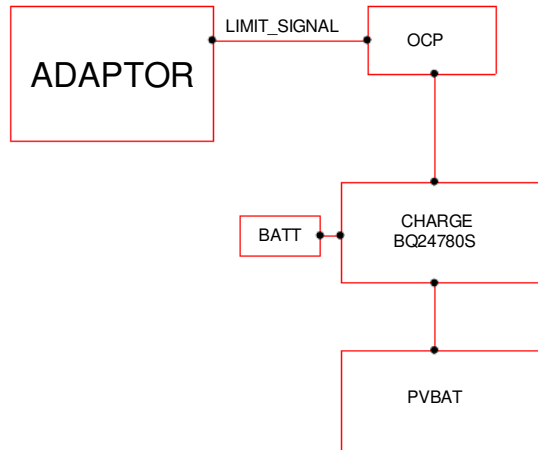
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TITLE			
MODEL PROJECT.FUNCTION			
TABLE OF I2C			
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SHEET	4	of 101	

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

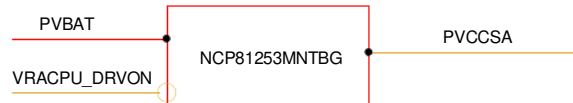
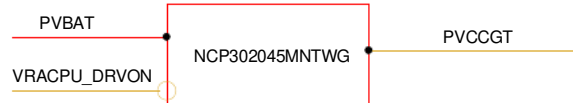
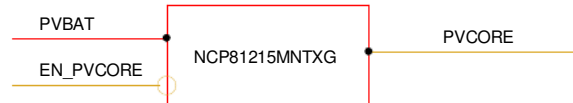
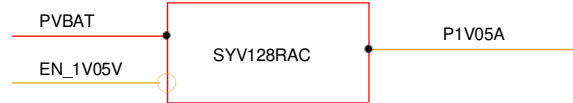
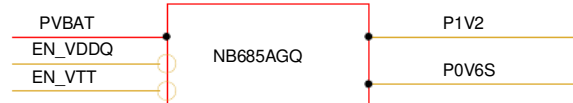


# POWER BLOCK



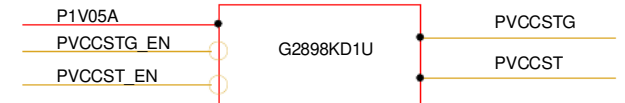
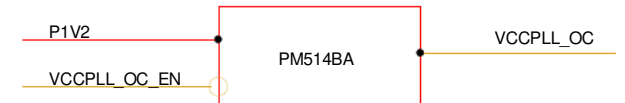
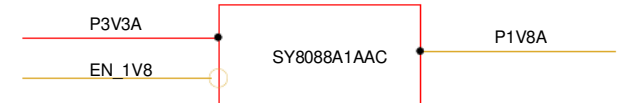
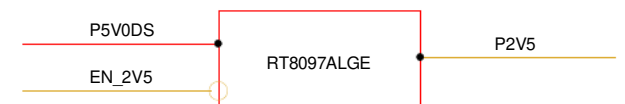
## IN/EN

## OUT



## IN/EN

## OUT



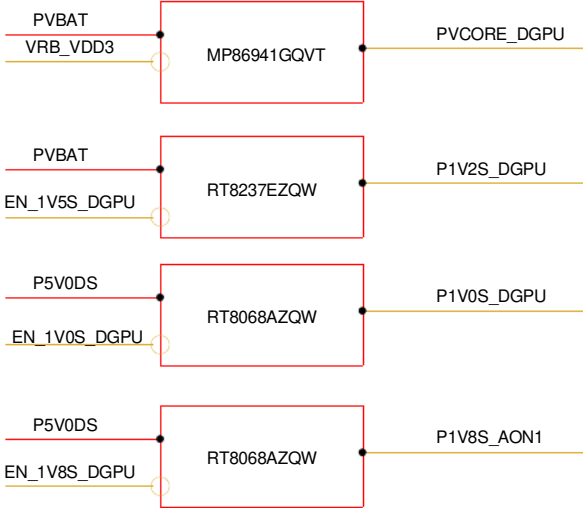
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MODEL PROJECT FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
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CHANGE by PCB P/N	XXX 60xxxxxxxxxx	DATE PCB VER	21-OCT-2002 XXX
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# GPU POWER BLOCK

IN/EN                      OUT

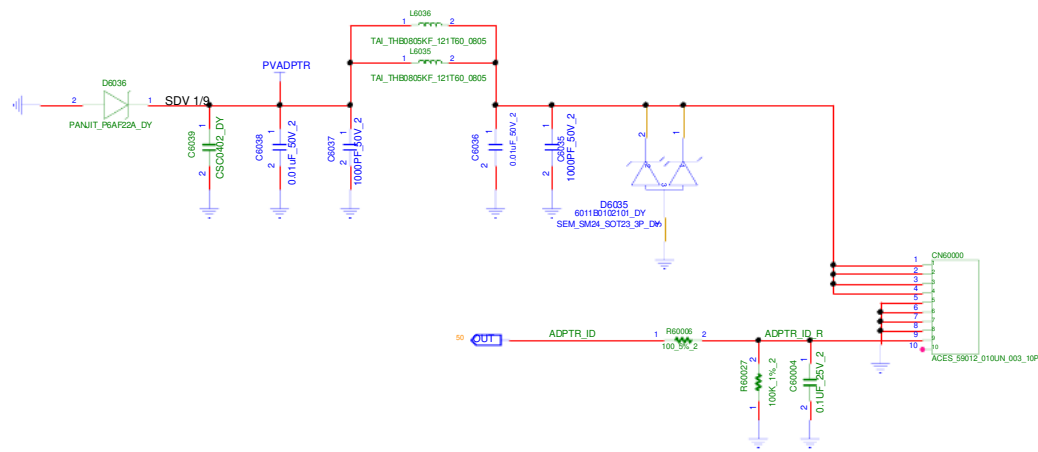


INVENTEC

TITLE  
MODEL PROJECT FUNCTION  
TABLE OF I2C

SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 6	of 101		

CHANGE by PCB P/N	XXX 60xxxxxxxxxx	DATE PCB VER	21-OCT-2002 XXX
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**INVENTEC**

TITLE			
MODEL_PROJECT.FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310000000000	001
SHEET	7	of 10	

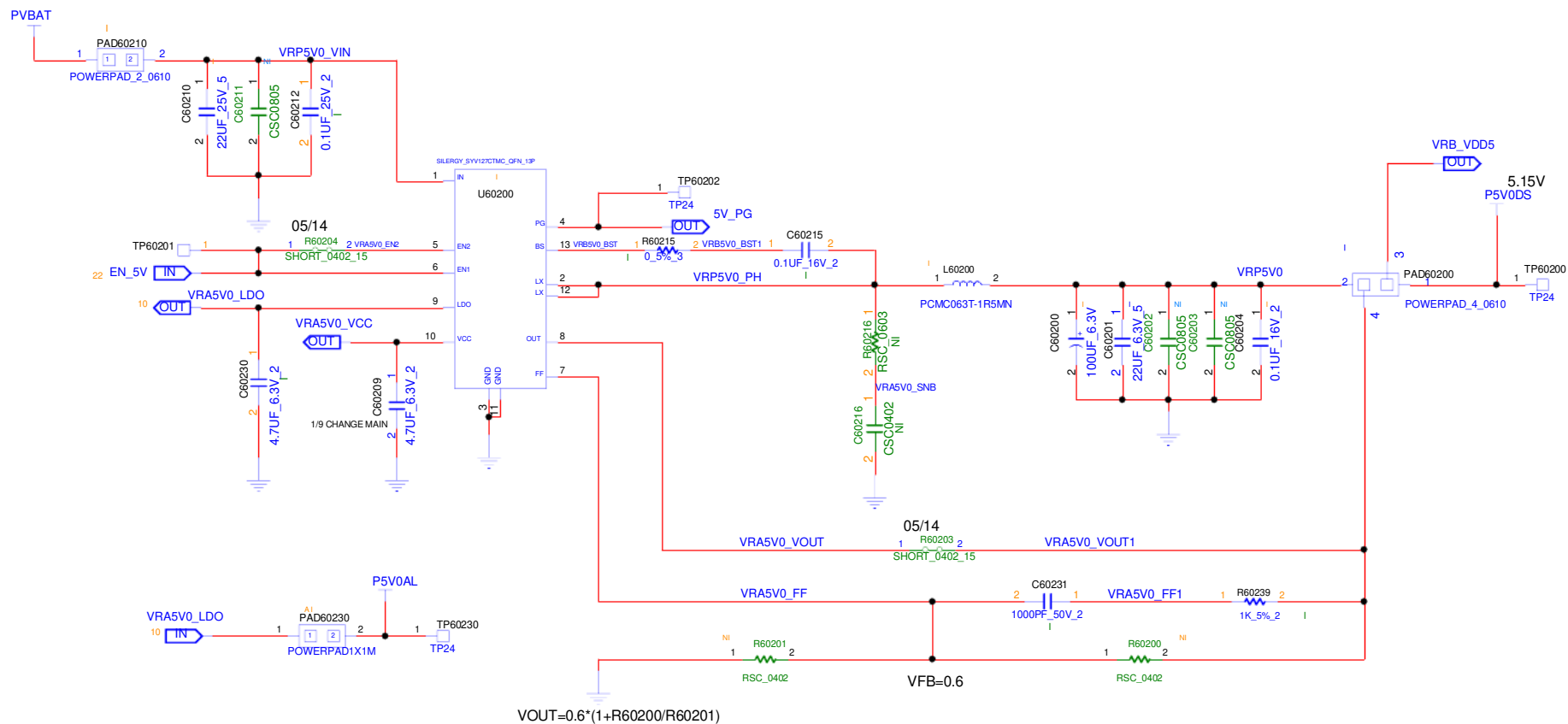
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PCB P/N XXX	21-OCT-2002
PCB VER XXX	



## F

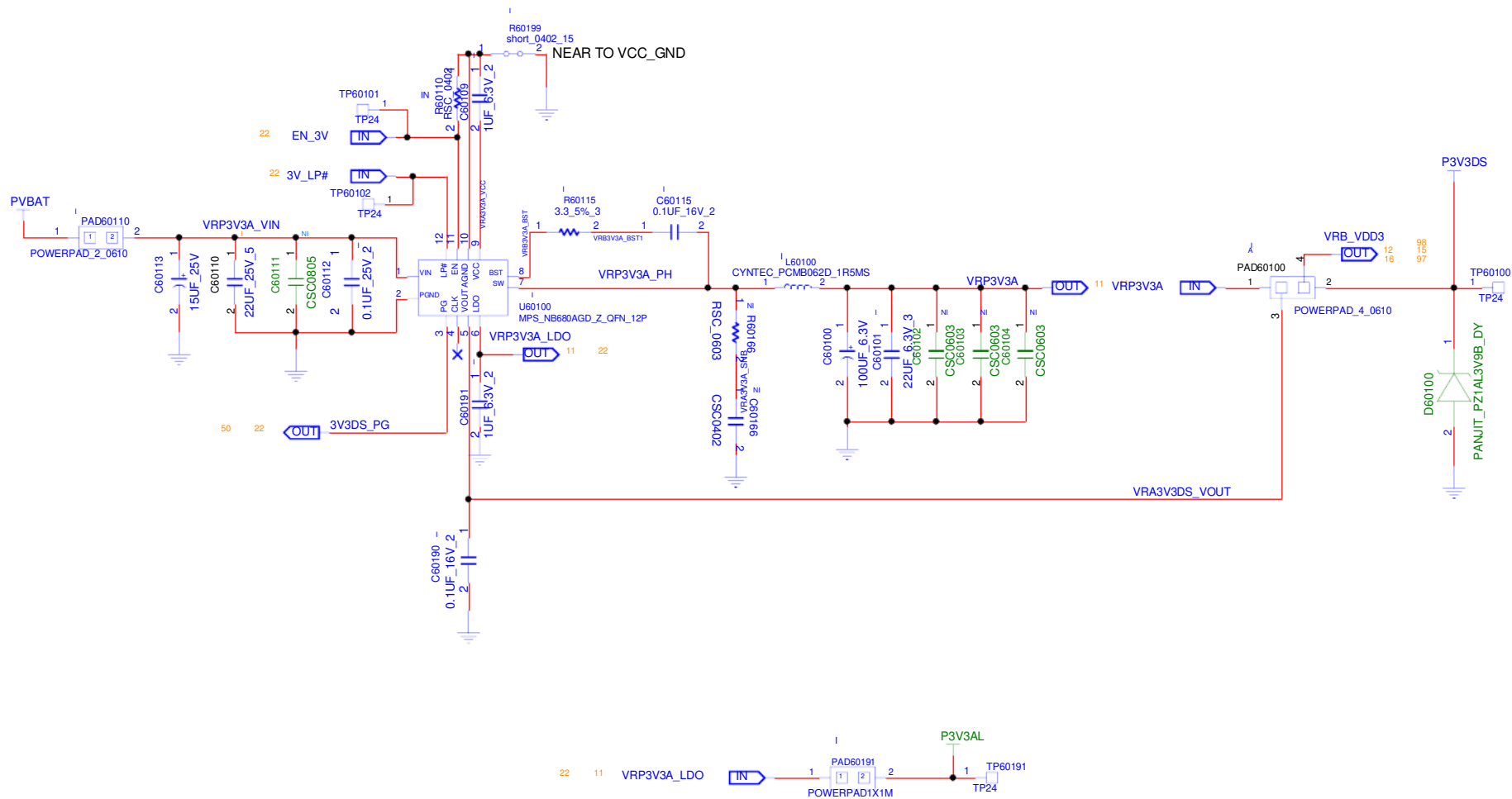
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TITLE	MODEL,PROJECT,FUNCTION Block Diagram
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$$V_{OUT}=0.6*(1+R_{60200}/R_{60201})$$

# INVENTEC

TITLE			
P5V0_NB679 (RIGHT SIDE FOR USB PORT)			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET		10 of 101	

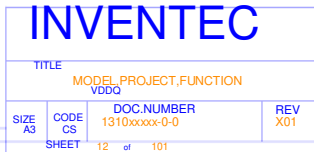


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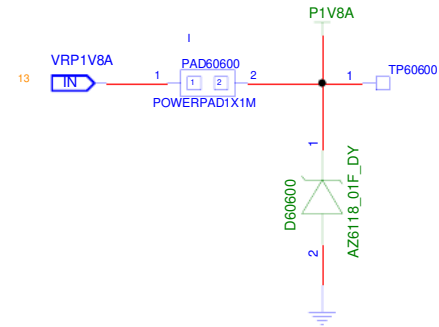
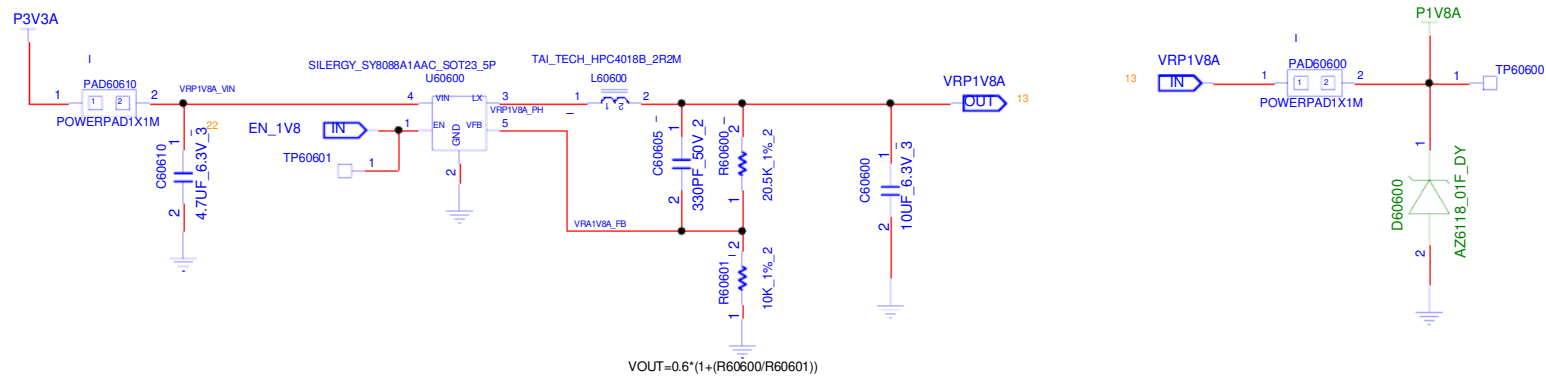
TITLE			
MODEL PROJECT FUNCTION P3V3DS_NB680A			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET		11 of 101	

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxx	PCB VER	XXX

State	EN1	EN2	VDDQ	VTTREF	VTT
S0	High	High	ON	ON	ON
S3	Low	High	ON	ON	OFF(High-Z)
S4/S5	Low	Low	OFF	OFF	OFF
Others	High	Low	OFF	OFF	OFF







INVENTEC

TITLE  
MODEL PROJECT FUNCTION  
P1V8DS

SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET		13 of 101	

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxx	PCB VER	XXX



SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
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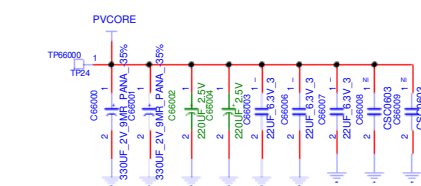
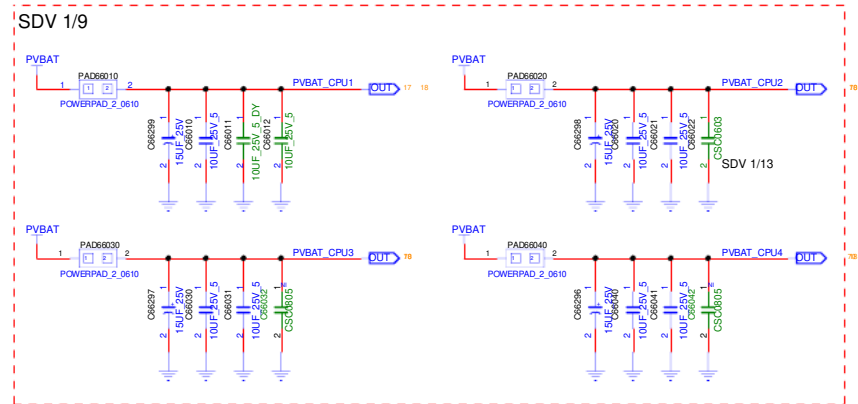
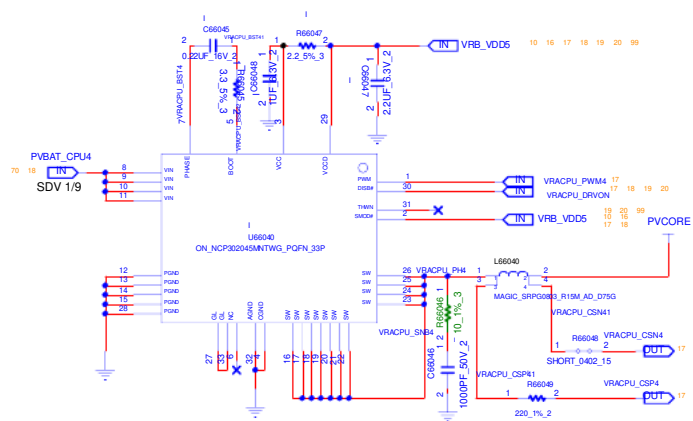
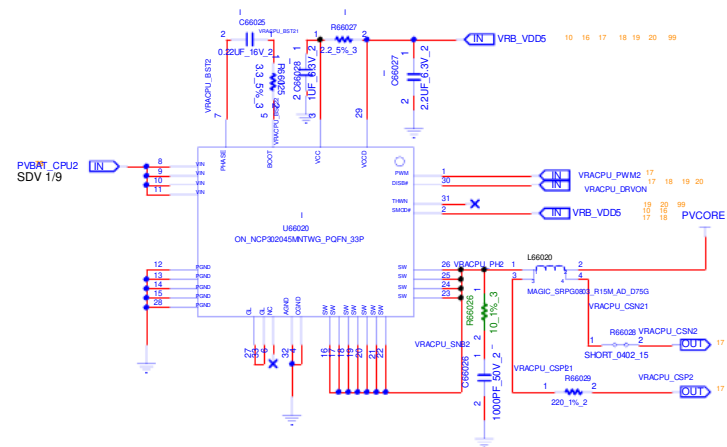
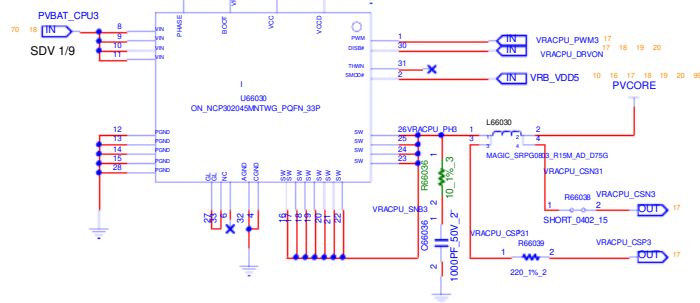
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

	LP#	C1	C0	VOUT(V)
<b>VCCIO</b>	0	X	X	0
	1	0	0	0.85
	1	0	1	0.875
	1	1	0	0.95
	1	1	1	0.975
<b>VCCPRIM _CORE</b>	0	X	X	0.75
	1	0	0	0.9
	1	0	1	0.95
	1	1	0	1.0
	1	1	1	1.05
<b>EDRAM/ EOPIO/ V1.0A</b>	0	X	X	0
	1	0	0	0.8 (MSM)
	1	0	1	0.95
	1	1	0	1
	1	1	1	1.05
<b>Others</b> (Fixed design only, not allowed for changing on-the-fly)	0	0	0	1.59
	0	0	1	1.99
	0	1	0	2.38
	0	1	1	3.3
	1	0	0	1.2
	1	0	1	1.5
	1	1	0	1.8
	1	1	1	2.5



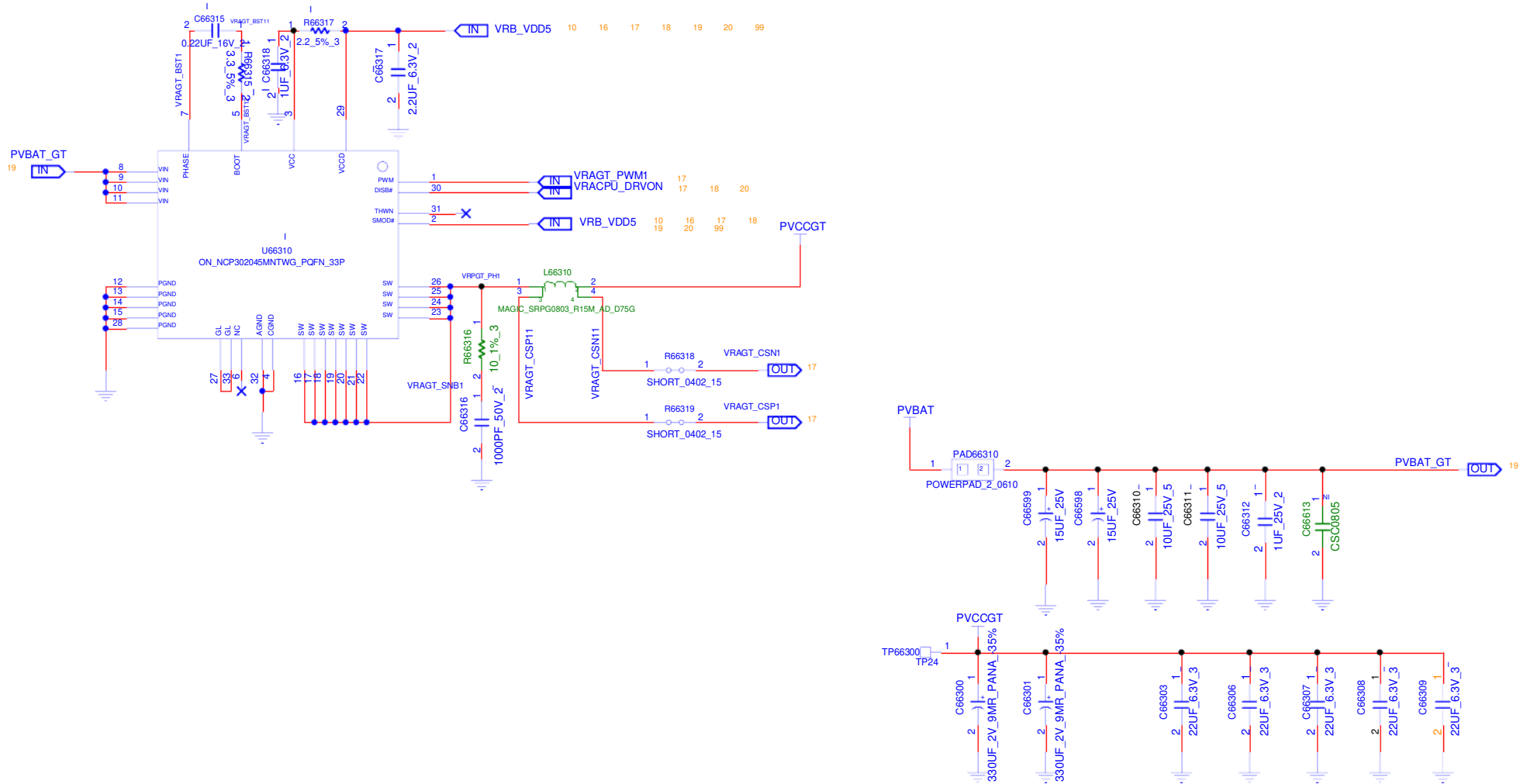
SIZE A3	CODE CS	DOC. NUMBER 1310xxxxx-0-0	REV X01
SHEET		16 of 101	





# CML-H82 45W BASELINE

TDC=25A  
ICCMAX=32A



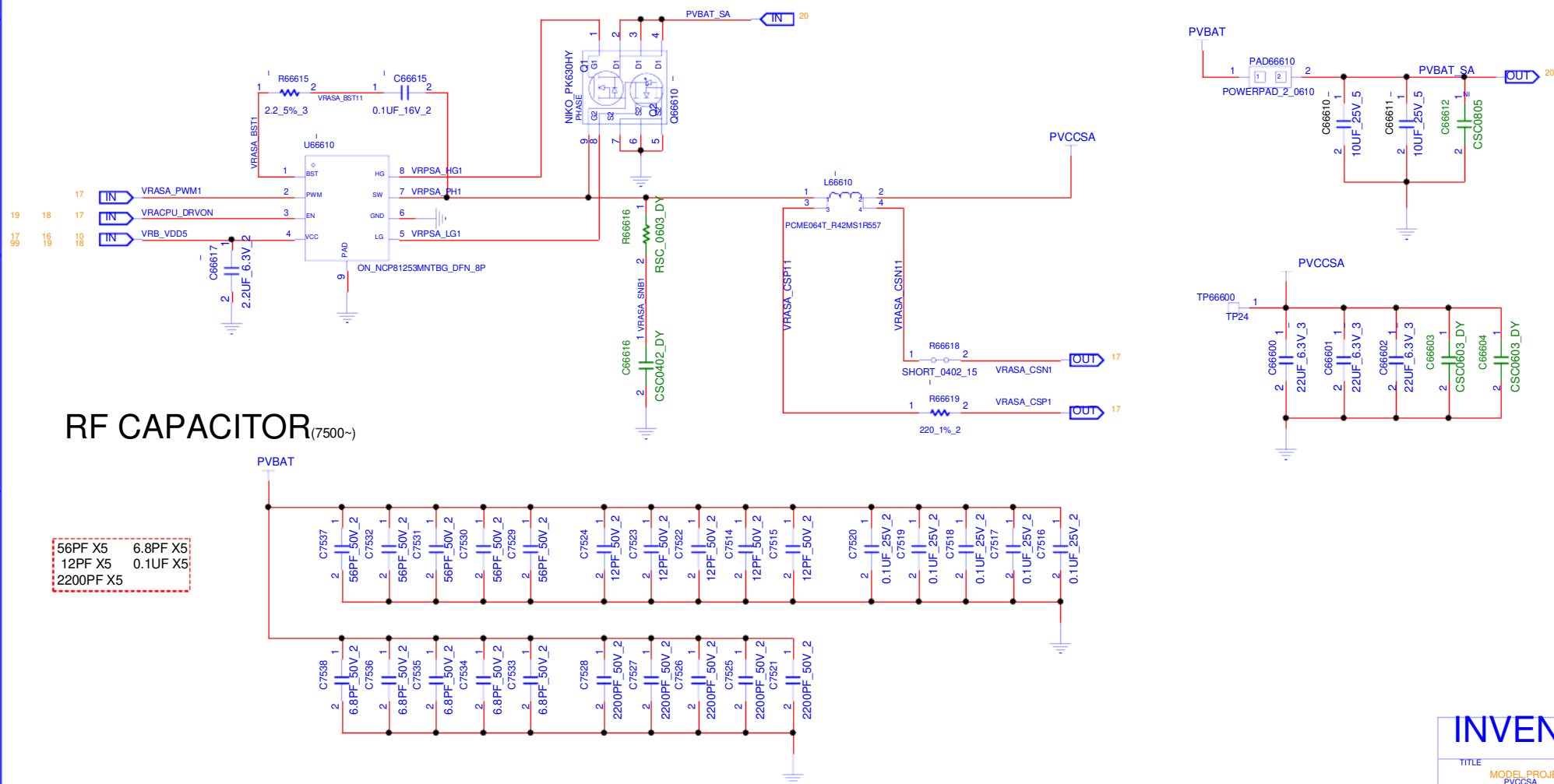
## INVENTEC

TITLE  
MODEL PROJECT.FUNCTION  
PVC001

SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
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CHANGE by PCB P/N	XXX 60xxxxxxxxxx	DATE PCB VER	21-OCT-2002 XXX
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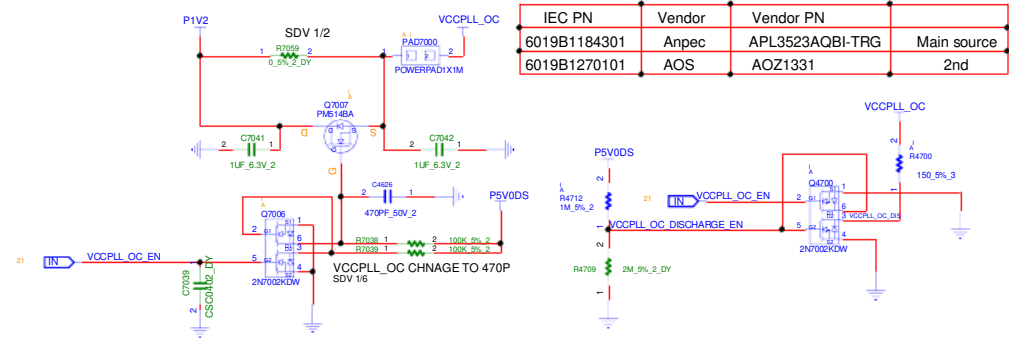
19 of 101



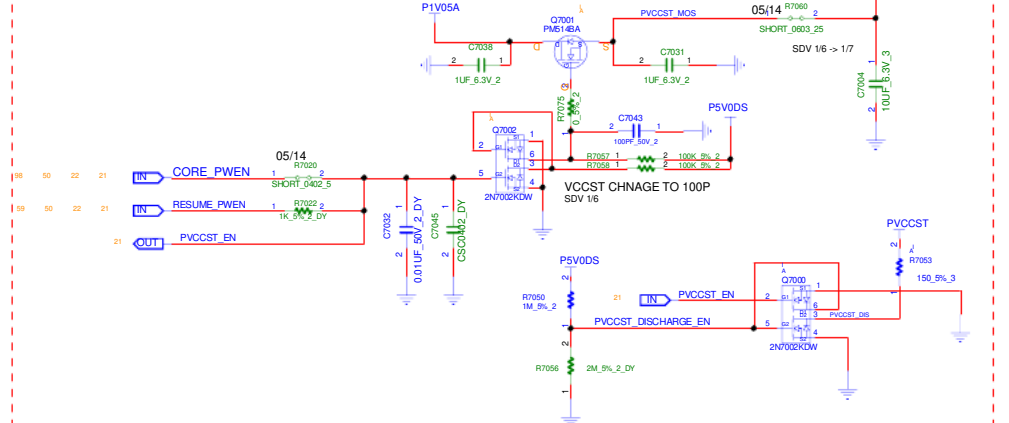
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TITLE			
MODEL,PROJECT,FUNCTION PVCCSA			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
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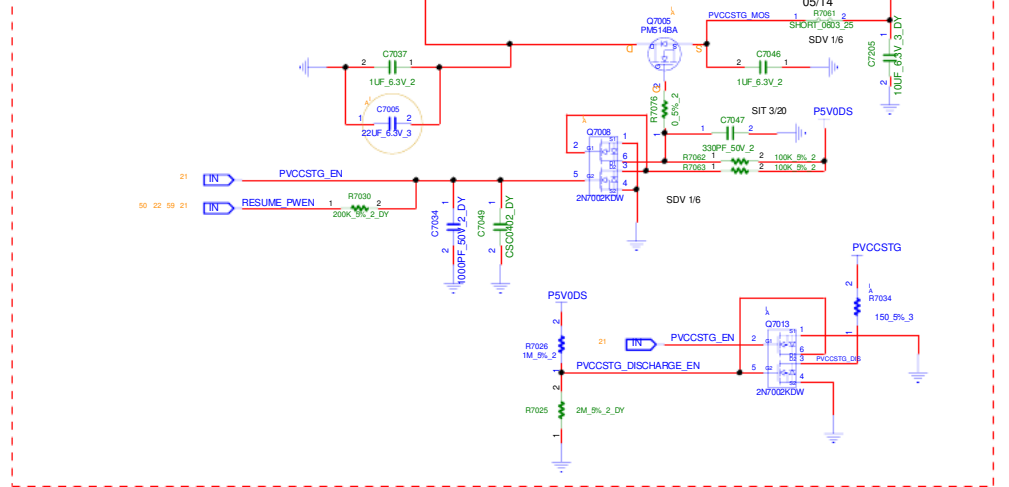




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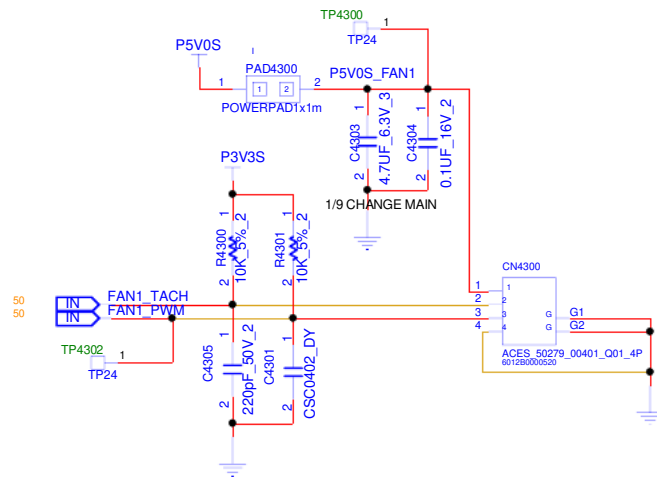


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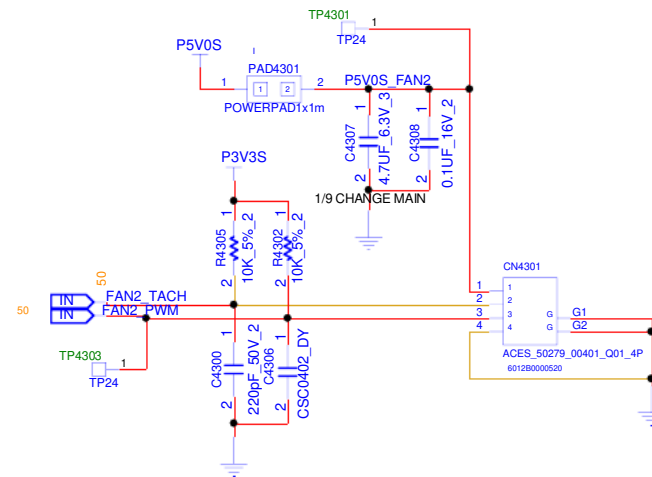




REFERENCE 4300~4349(FAN)  
REFERENCE 4411~4449(THERMAL)



FAN1 CN GPU



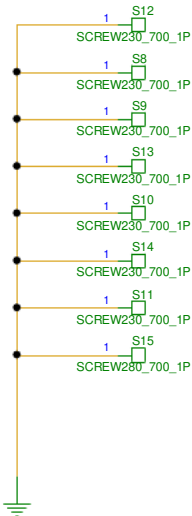
FAN2 CN CPU

INVENTEC

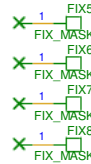
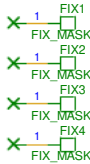
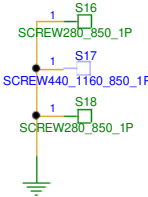
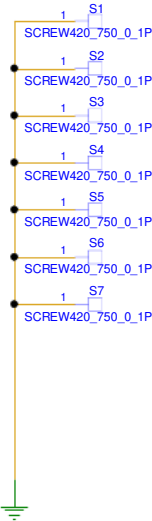
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MODEL PROJECT FUNCTION FAN & THERMAL			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 23 of 101			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

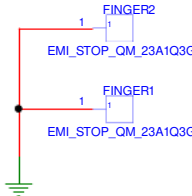
REFERENCE 0~49(PCB SCREW)



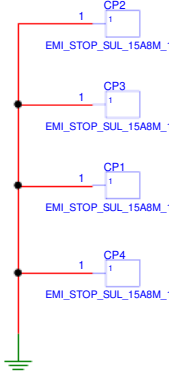
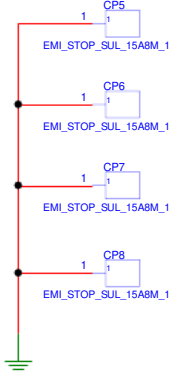
GPU CPU



SHIELDING SDV 1/9



DDR SHIELDING



INVENTEC

TITLE MODEL PROJECT FUNCTION XDP & ME CONN

SIZE CODE DOC NUMBER REV  
A3 CS 1310xxxx-0-0 X01  
SHEET 24 of 101

CHANGE by XXXX  
PCB P/N 60xxxxxxxxxx

DATE 21-OCT-2002  
PCB VER XXXX

D

C

B

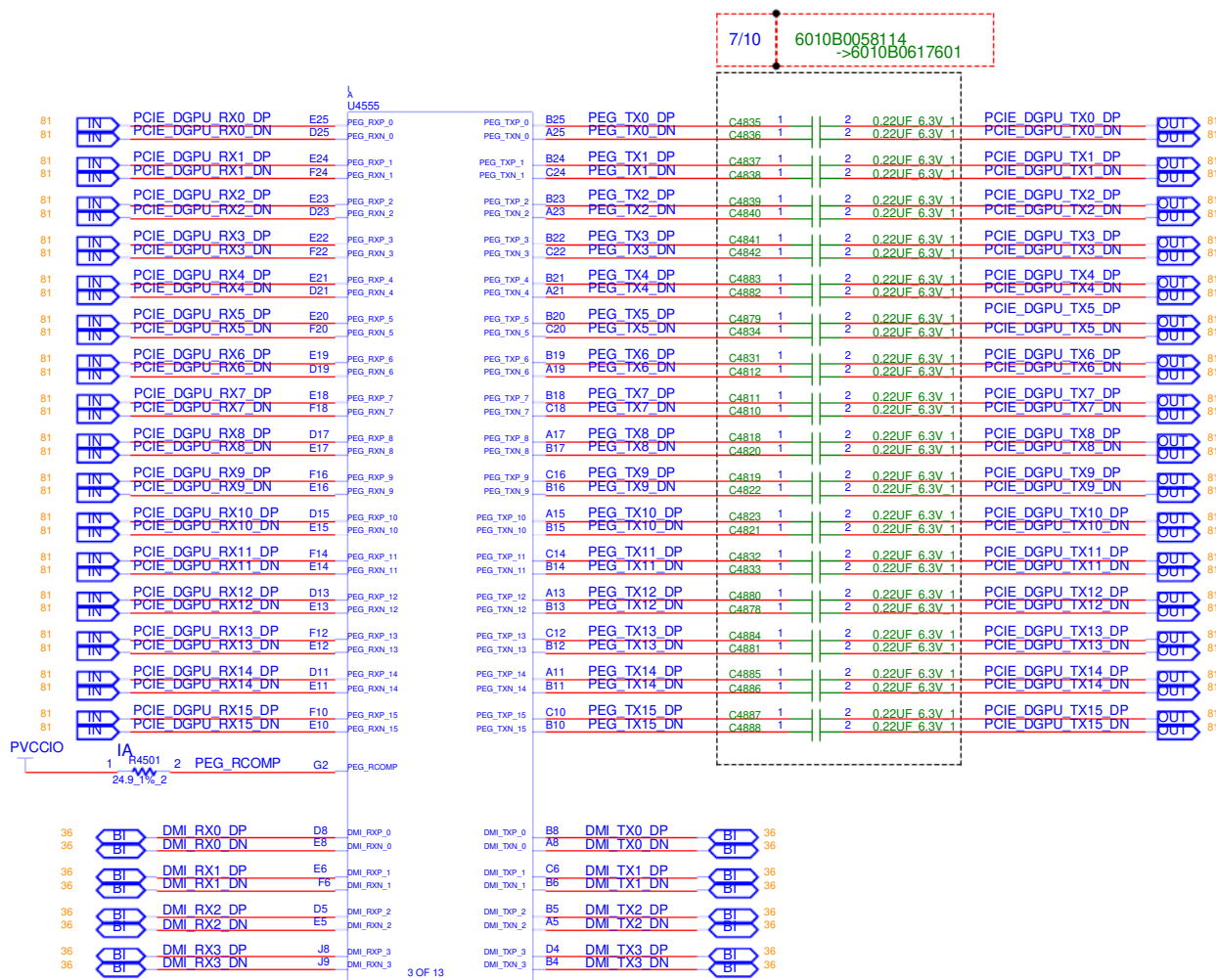
A

D

C

B

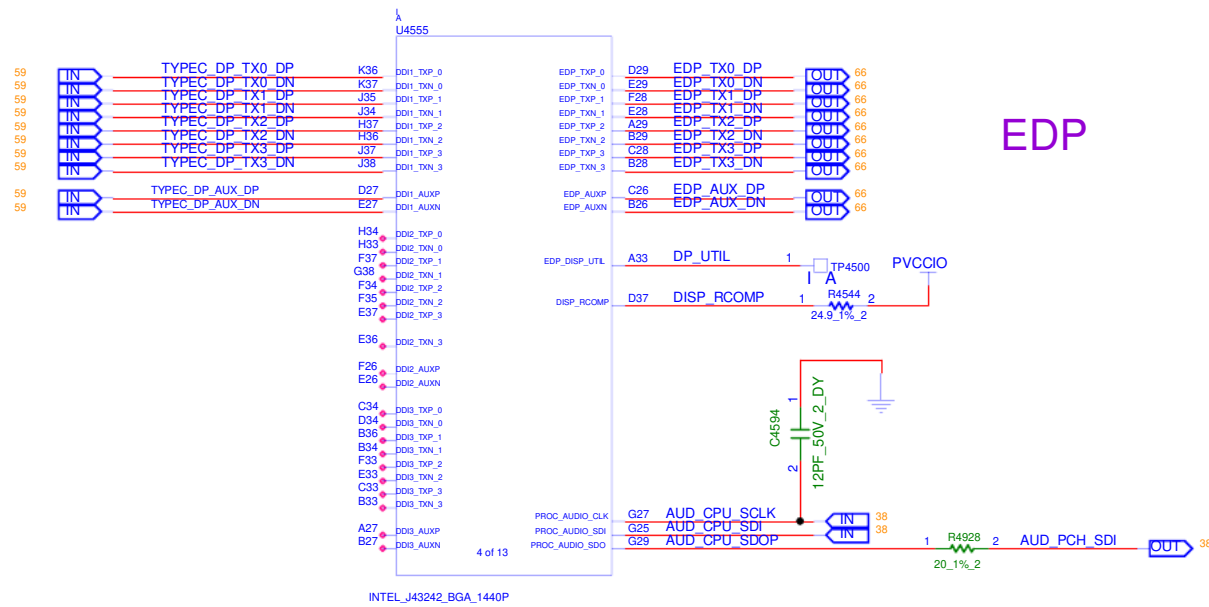
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INVENTEC

TITLE  
MODEL PROJECT FUNCTION  
SKYLAKE1\_H-PEG-HDMI

SIZE CODE DOC NUMBER REV  
A3 CS 1310xxxx-0-0 X01  
SHEET 25 of 101

**INVENTEC**TITLE  
MODEL PROJECT FUNCTION  
SKYLAKE2-H-DDI-EDP

SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET 26 of 101			

CHANGE by PCB P/N	XXX 60xxxxxxxxxxx	DATE PCB VER	21-OCT-2002 XXX
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D

C

B

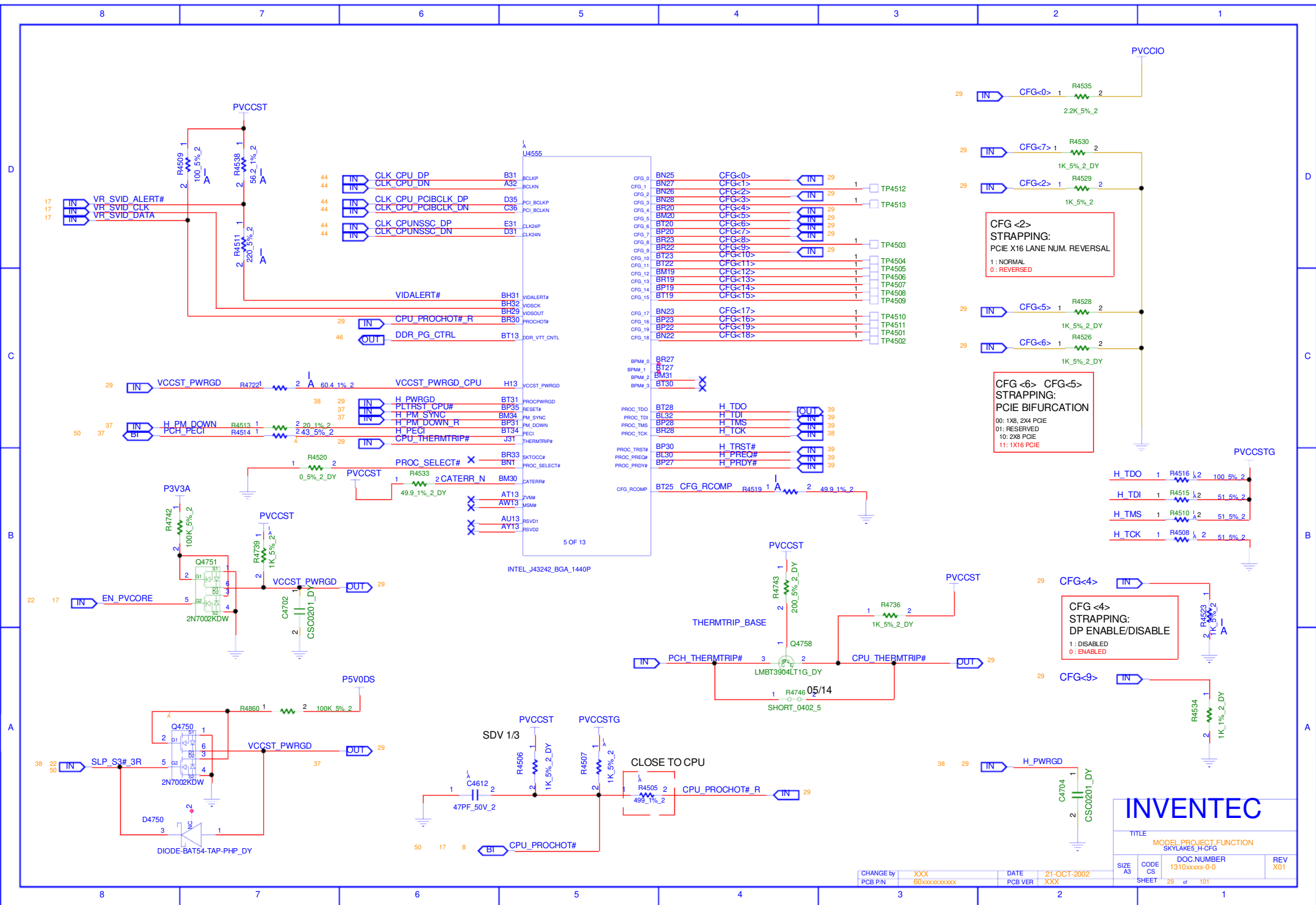
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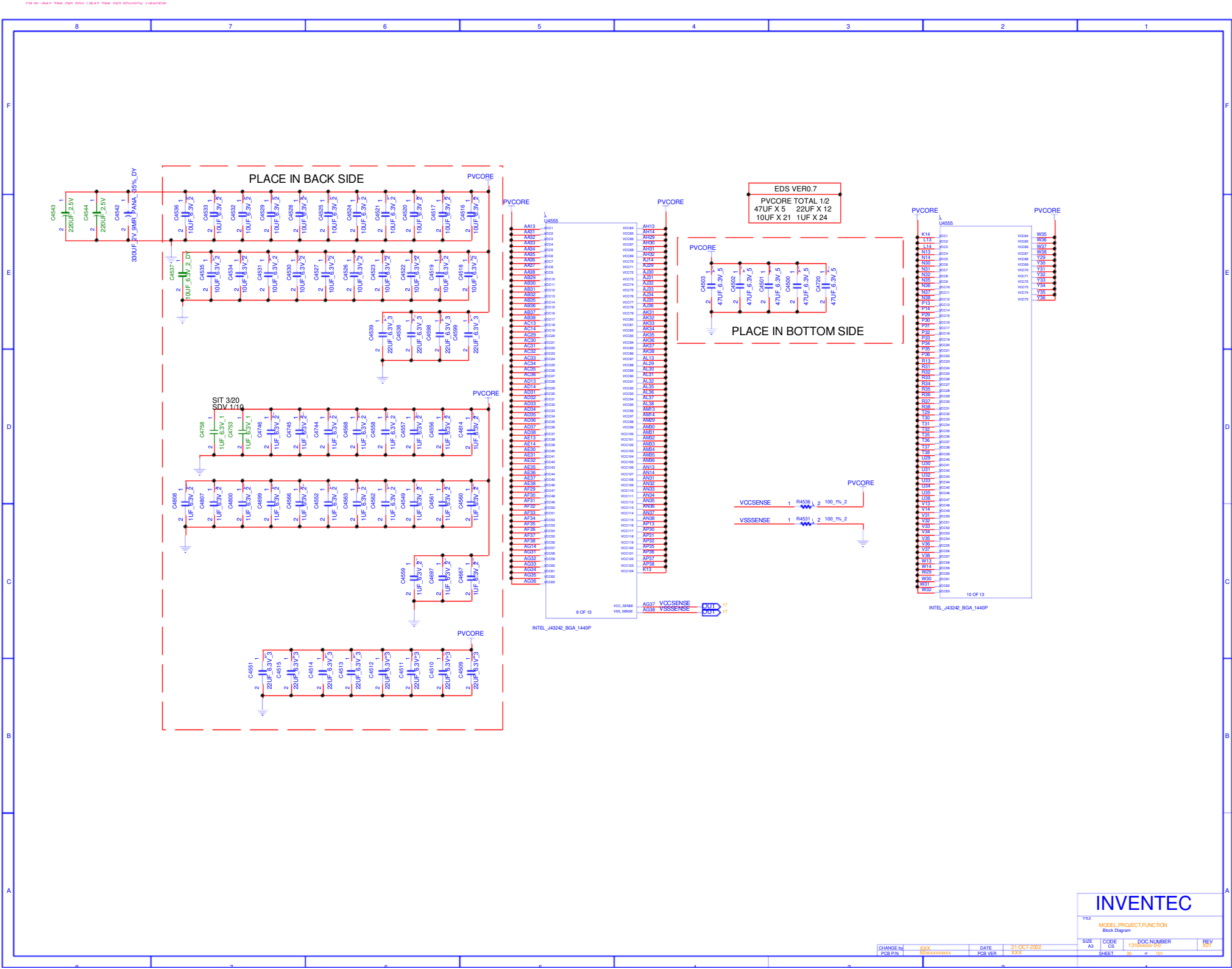
D

C

B

A

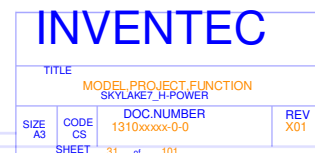


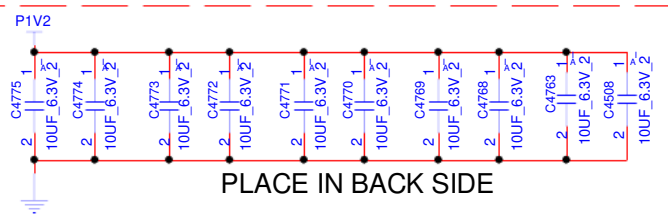
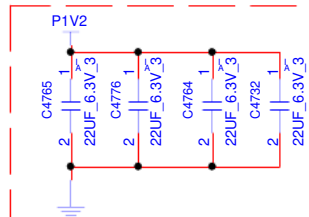


INVENTEC

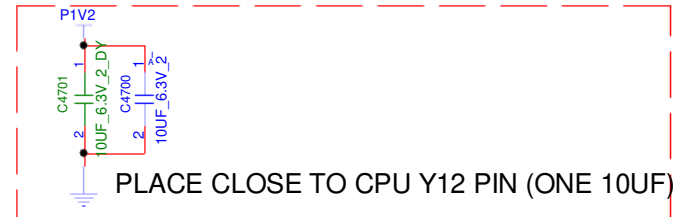
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MODEL_PROJECT_FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	131600000-000	001
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CHANGE NO	XXX	DATE	21-OCT-2002
PCB P/N	800000000000	PCB VER	XXX

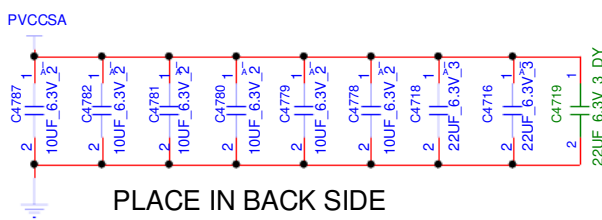
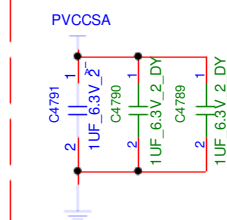




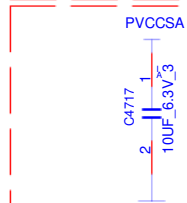
PLACE IN BACK SIDE



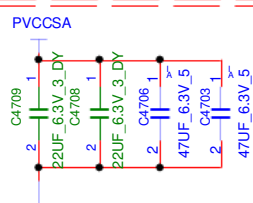
PLACE CLOSE TO CPU Y12 PIN (ONE 10UF)



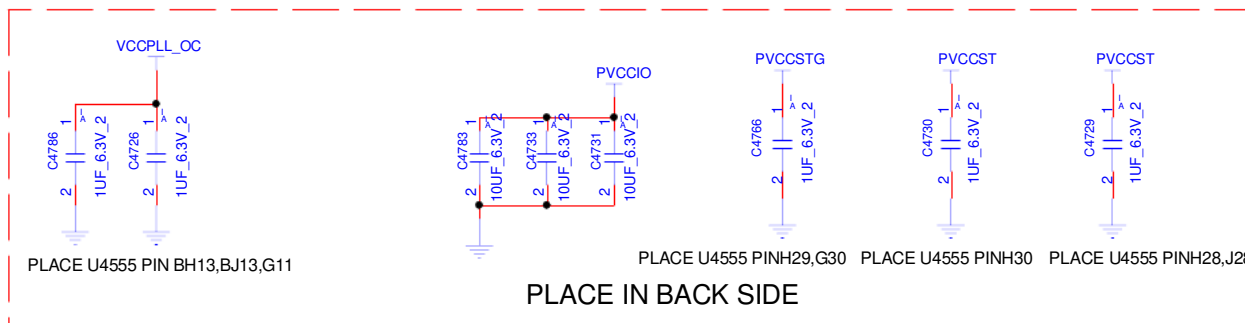
PLACE IN BACK SIDE



PLACE IN TOP SIDE



EDS VER0.7	
P1V2	
10UF X 11	22UF X 4
PVCCSA	
47UF X 2	22UF X 2
10UF X 7	1UF X 1



PLACE U4555 PIN BH13,BJ13,G11

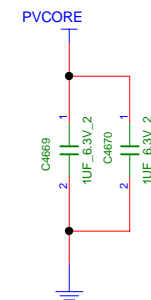
PLACE U4555 PINH29,G30 PLACE U4555 PINH30 PLACE U4555 PINH28,J28

PLACE IN BACK SIDE

INVENTEC

TITLE			
MODEL PROJECT FUNCTION SKYLAKES_H-DECOUPLING			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
SHEET	32	of 101	

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

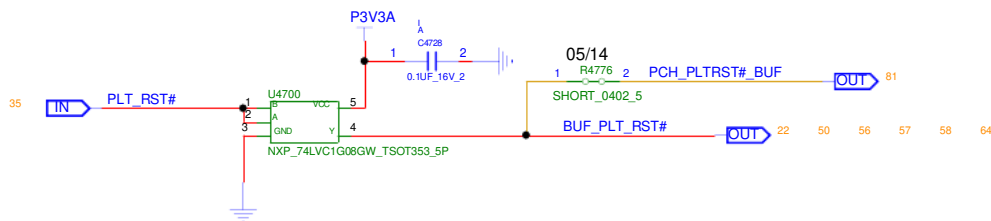
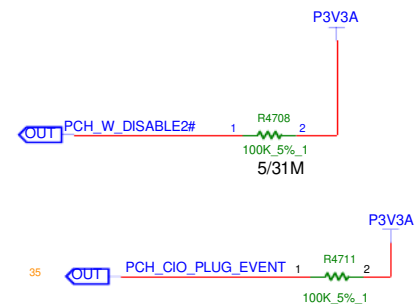


H82 CPU

SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 33 of 101			

SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 33 of 101			

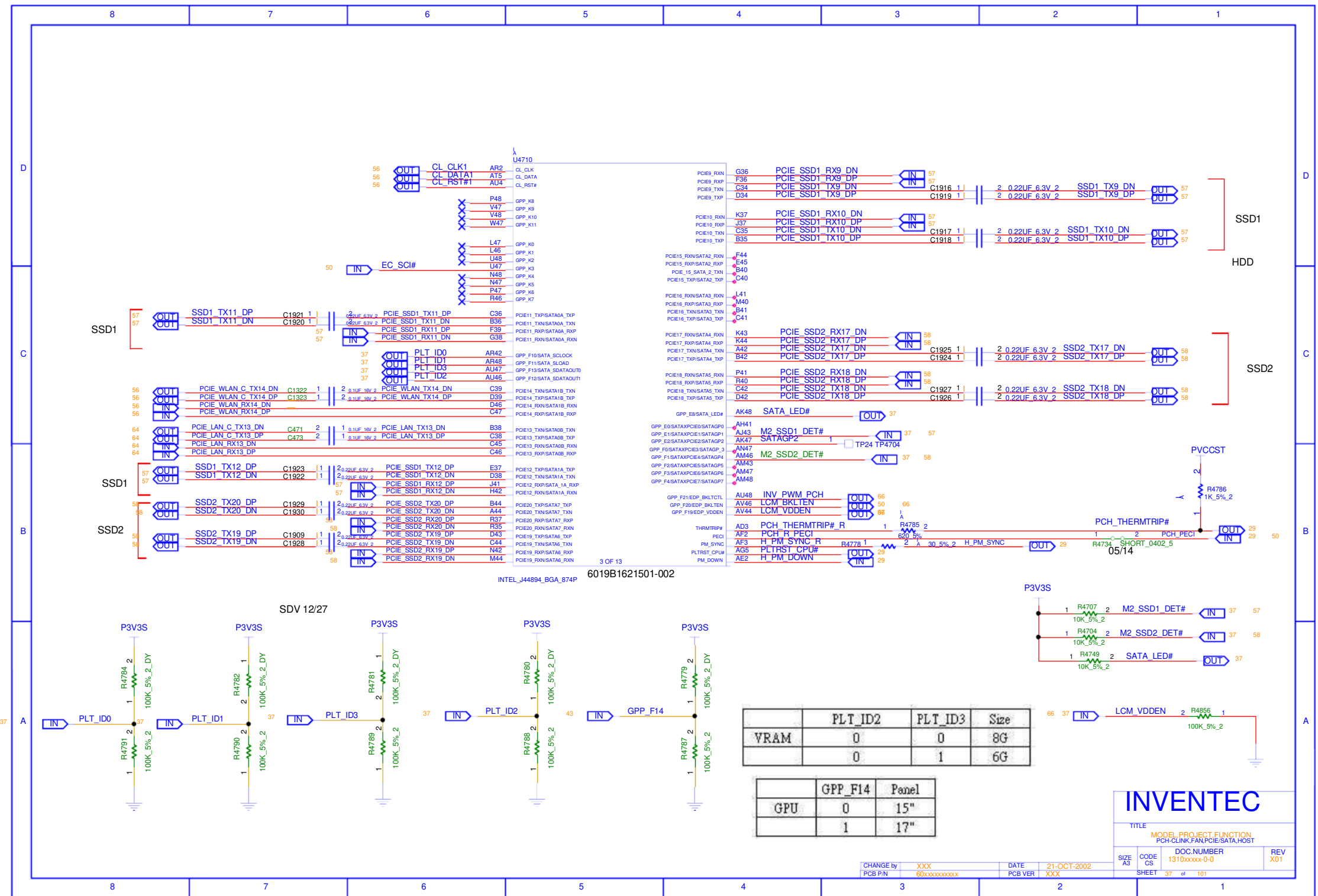


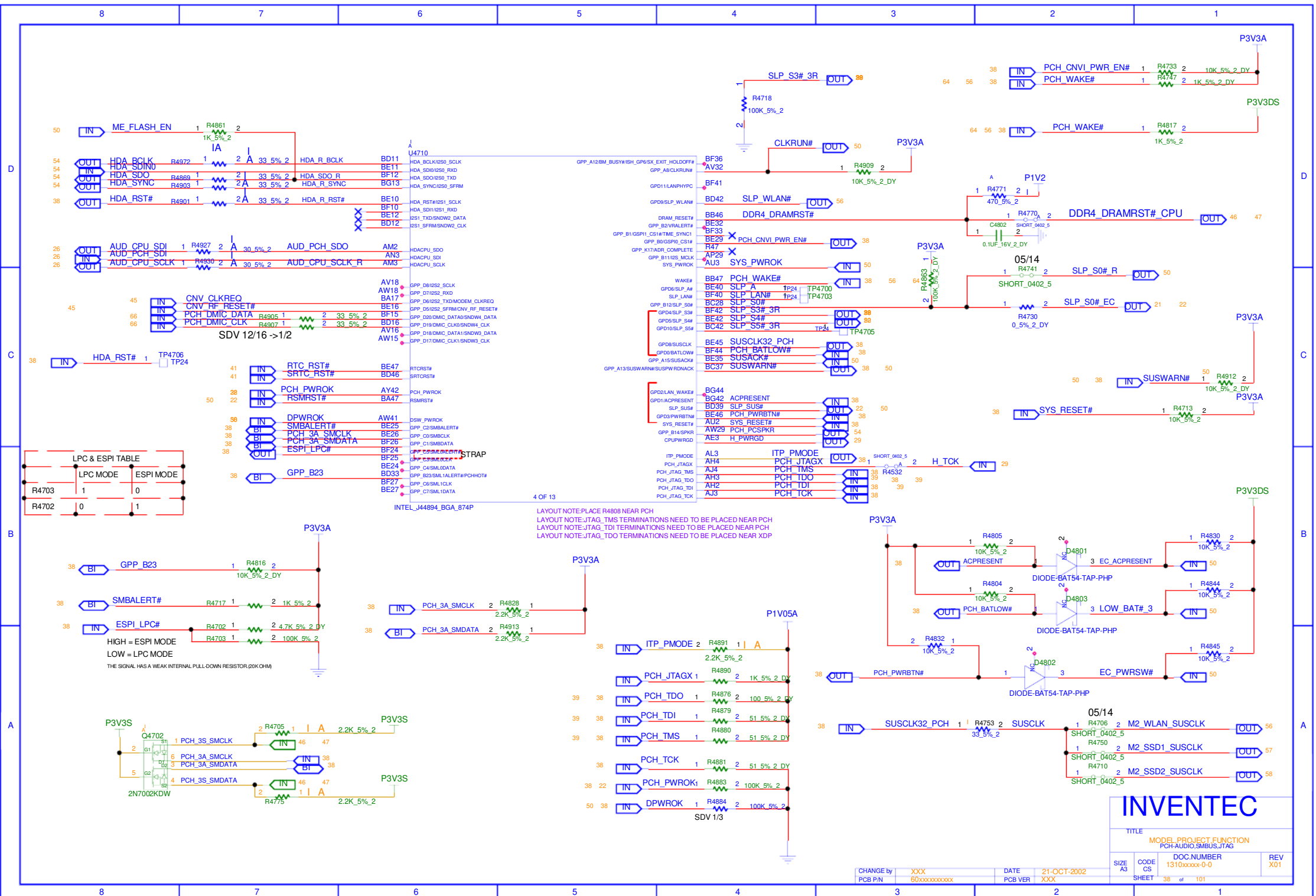


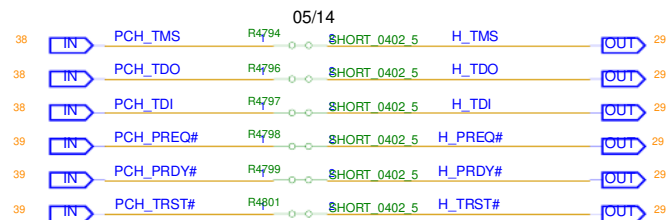
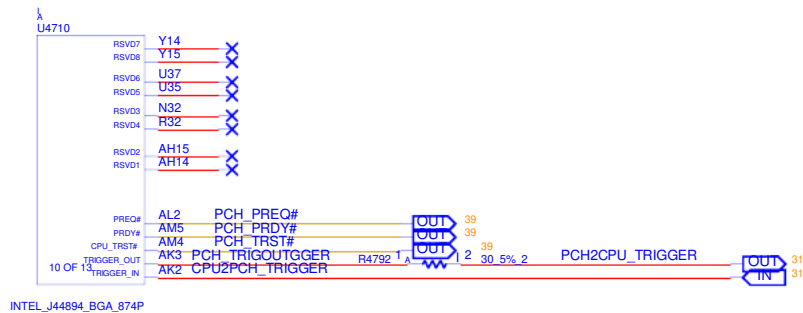
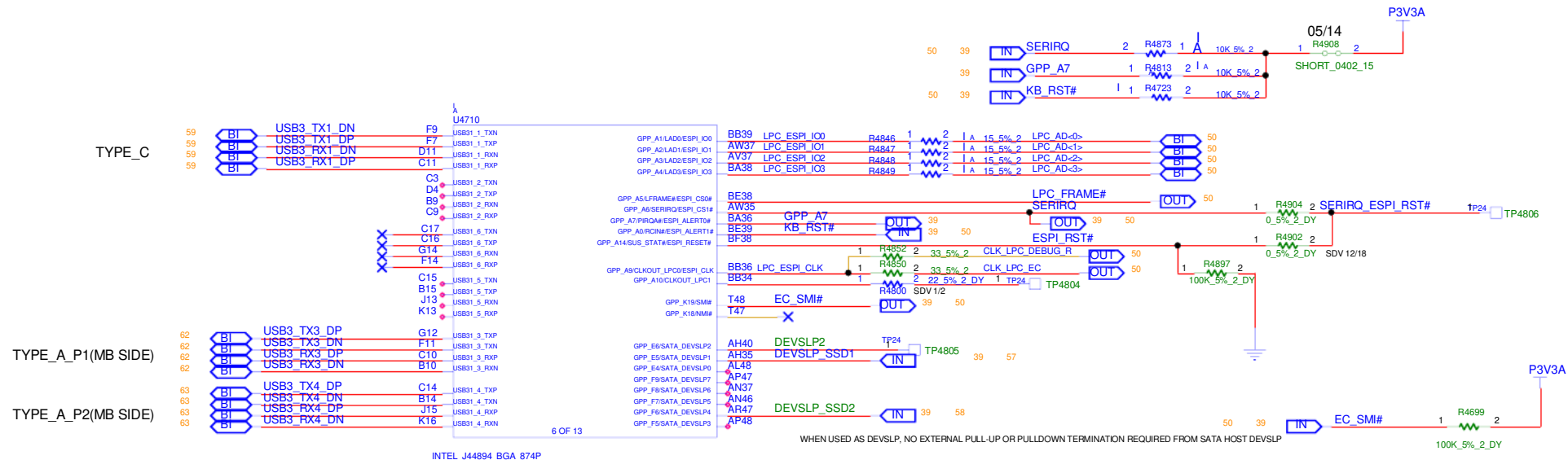
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET		35 of 101	



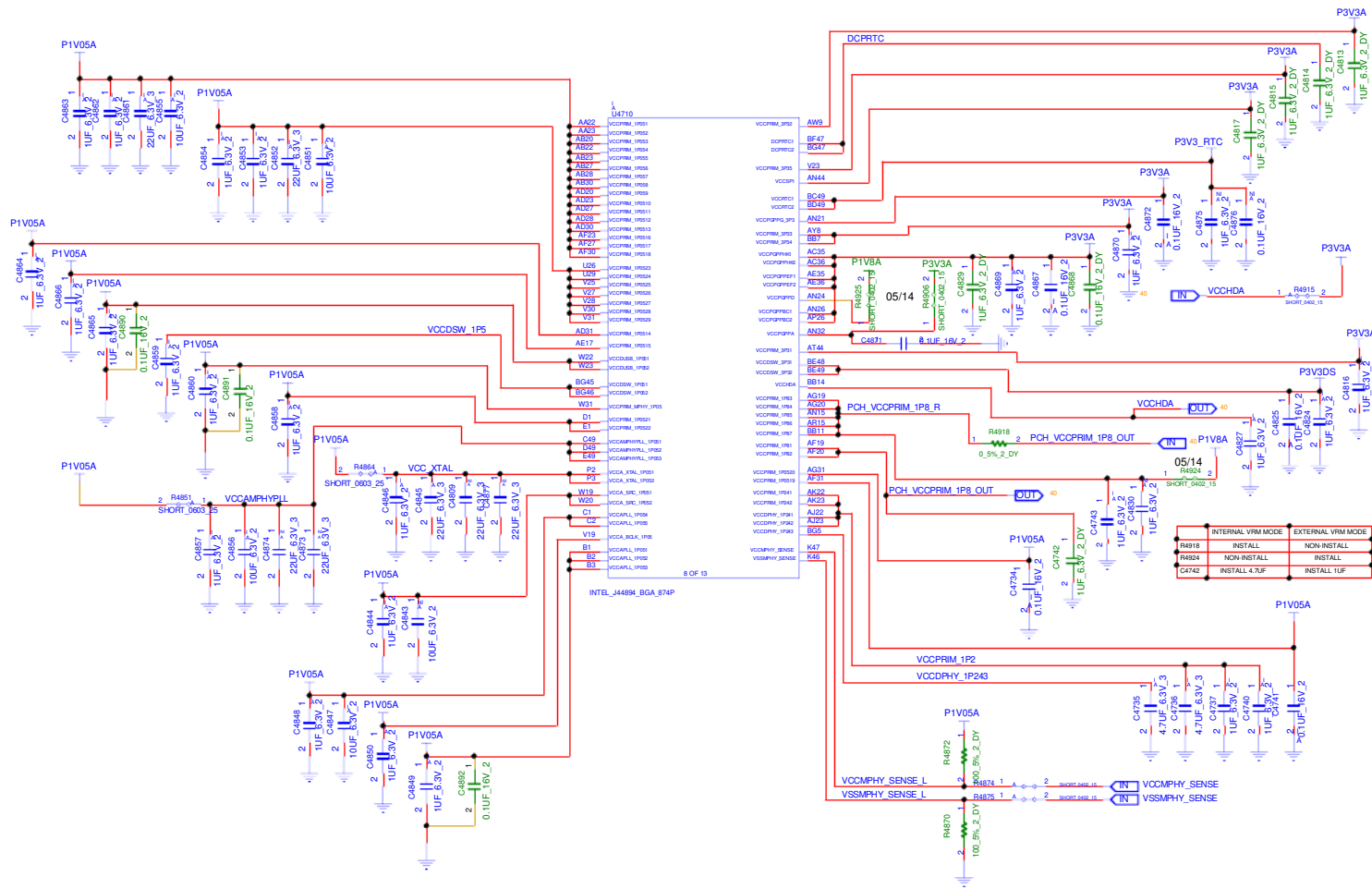




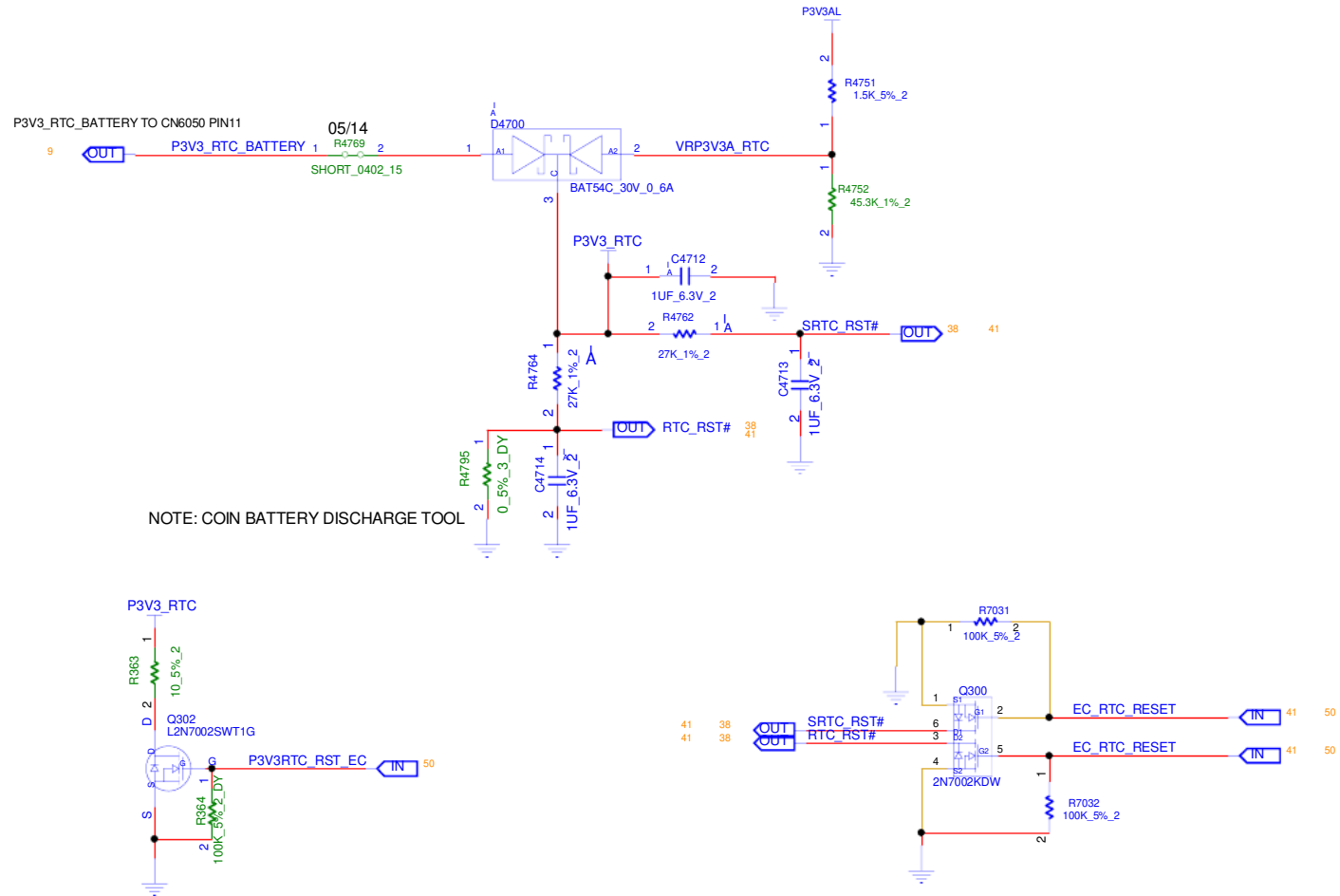


**INVENTEC**

TITLE			
MODEL PROJECT FUNCTION PCH/LPC/ESPI/USB/SATA			
SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
SHEET 39	of 101		



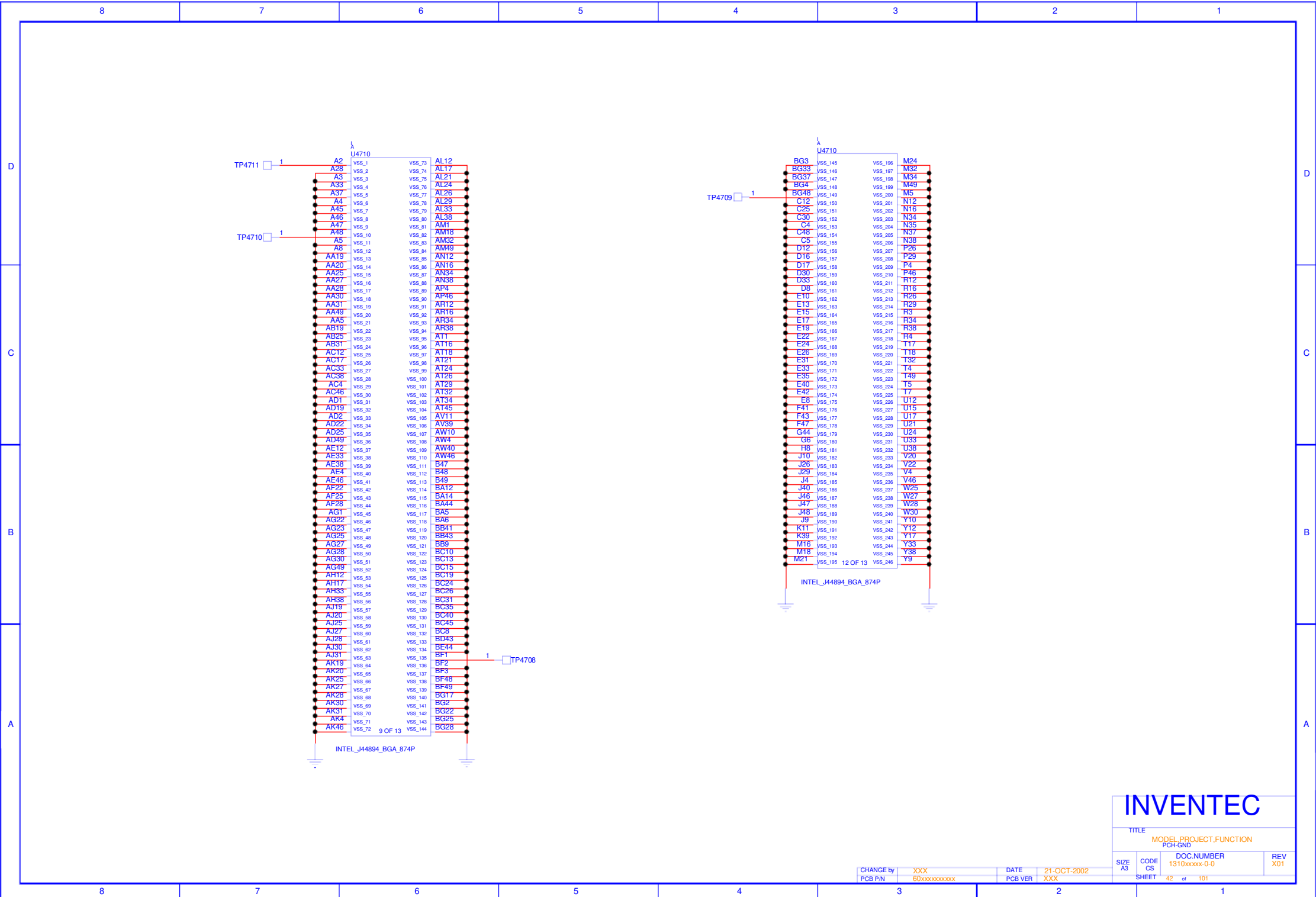
# RTC



## INVENTEC

TITLE			
MODEL PROJECT FUNCTION Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
SHEET		41 of 101	

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX



INVENTEC

TITLE  
MODEL PROJECT FUNCTION  
PCB GND

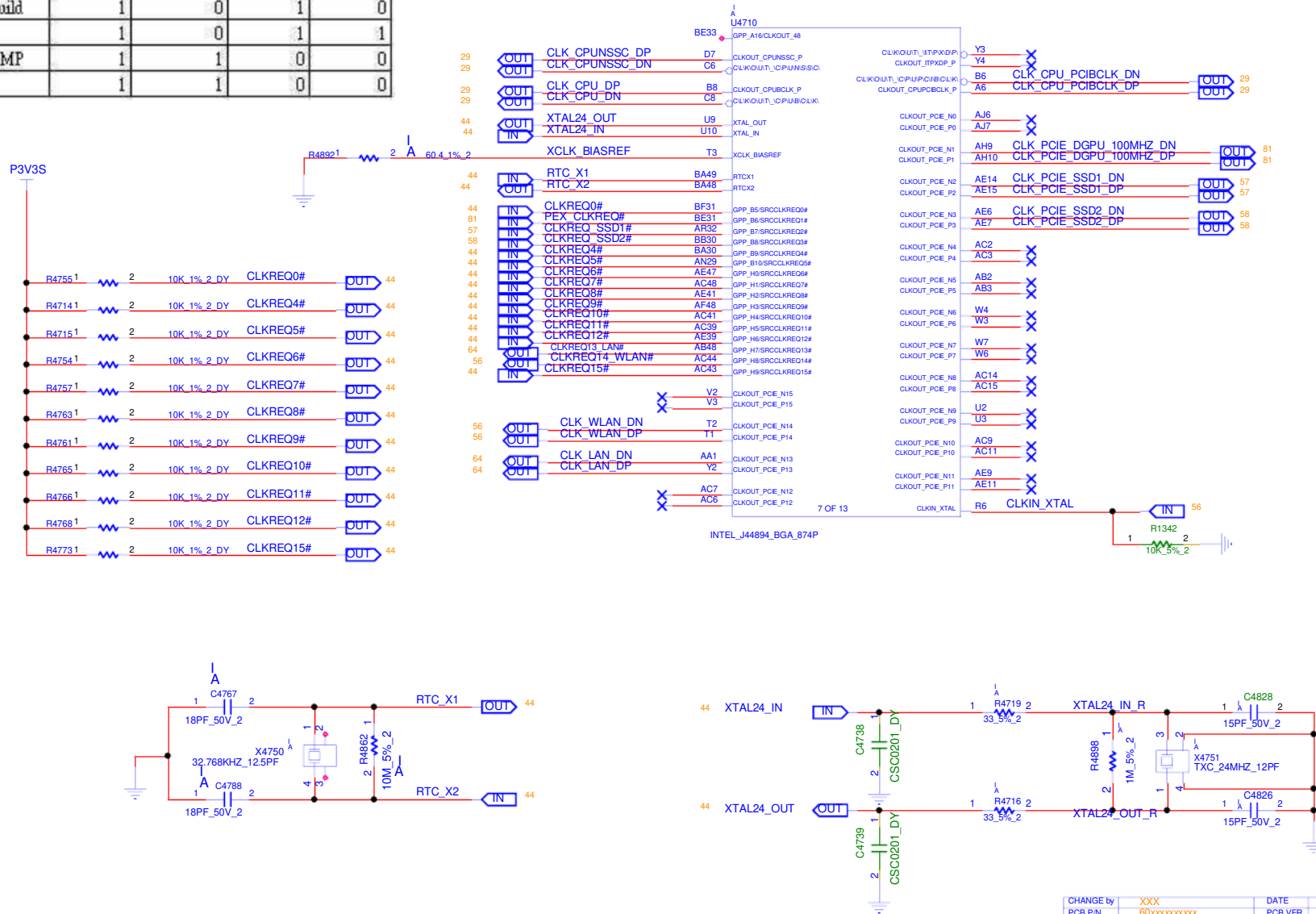
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET	42	of 101	

CHANGE by XXX  
PCB P/N 60xxxxxxxxx  
DATE 21-OCT-2002  
PCB VER XXX



	GPP_A23	GPP_A22	GPP_A21	GPP_A20
A build0	0	0	0	0
A build1	0	0	0	1
B build0	0	1	0	0
B build1	0	1	0	1
B build2	0	1	1	0
	0	1	1	1
C build0	1	0	0	0
	1	0	0	1
D build	1	0	1	0
	1	0	1	1
Pre-MP	1	1	0	0
MP	1	1	0	0

- SSC = Spread Spectrum Clocking
- The SRCCLKREQ#[15:0] signals can be configured to map to any of the PCH-H PCI Express\* Root Ports
- SRCCLKREQ#[15:0] to CLKOUT\_PCIE\_P/N[15:0] Mapping Requirements
  - SRCCLKREQ#[7:0] signals can be mapped to any of the CLKOUT\_PCIE\_P/N[7:0] differential clock pairs
  - SRCCLKREQ#[15:8] signals can be mapped to any of the CLKOUT\_PCIE\_P/N[15:8] differential clock pairs

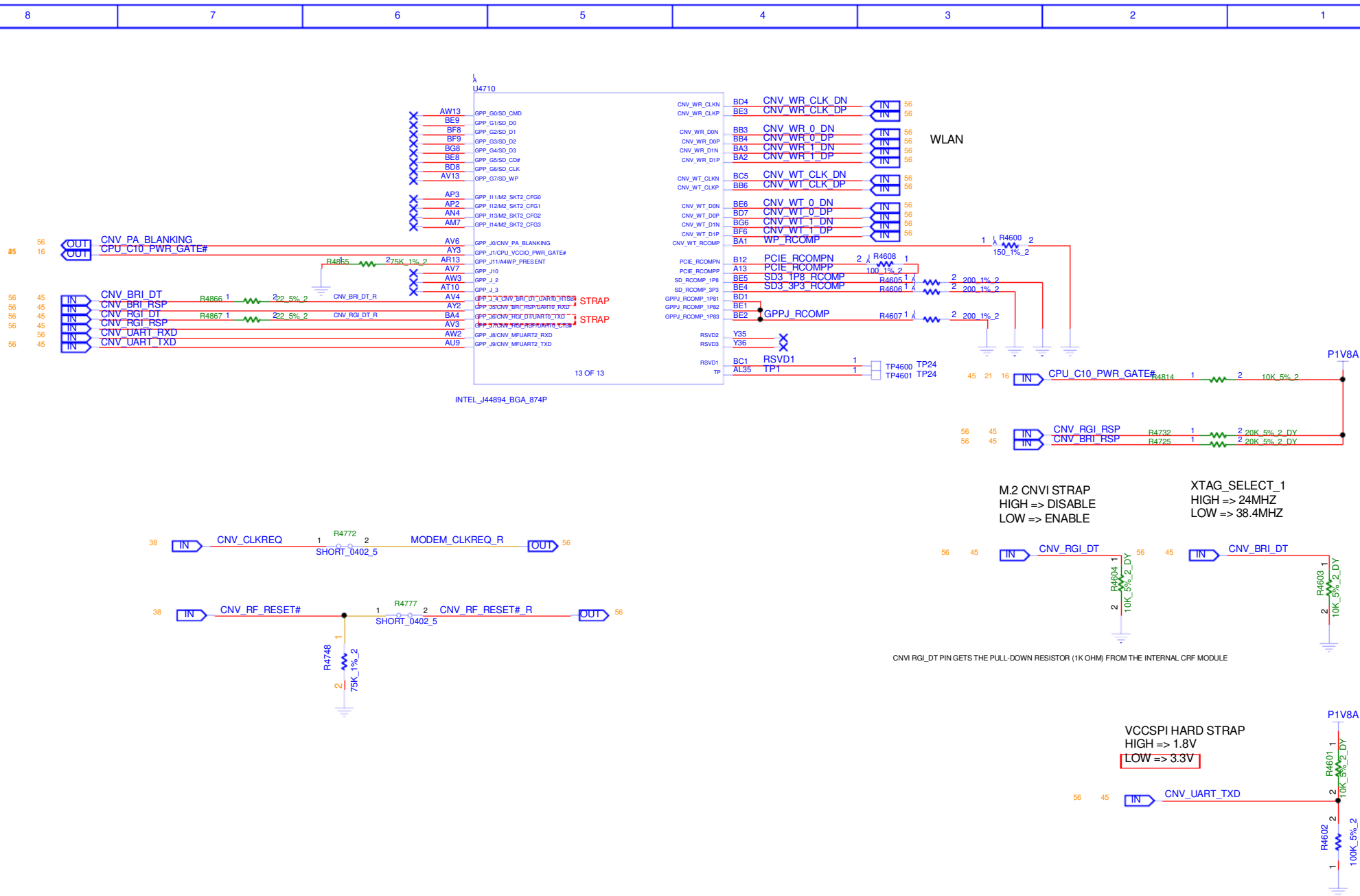


# INVENTEC

TITLE			
MODEL PROJECT FUNCTION			
PCH-GPP,CLKOUT			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET	44 of 101		

CHANGE by XXXX DATE 21-OCT-2002  
PCB P/N 60xxxxxxx PCB VER XXX

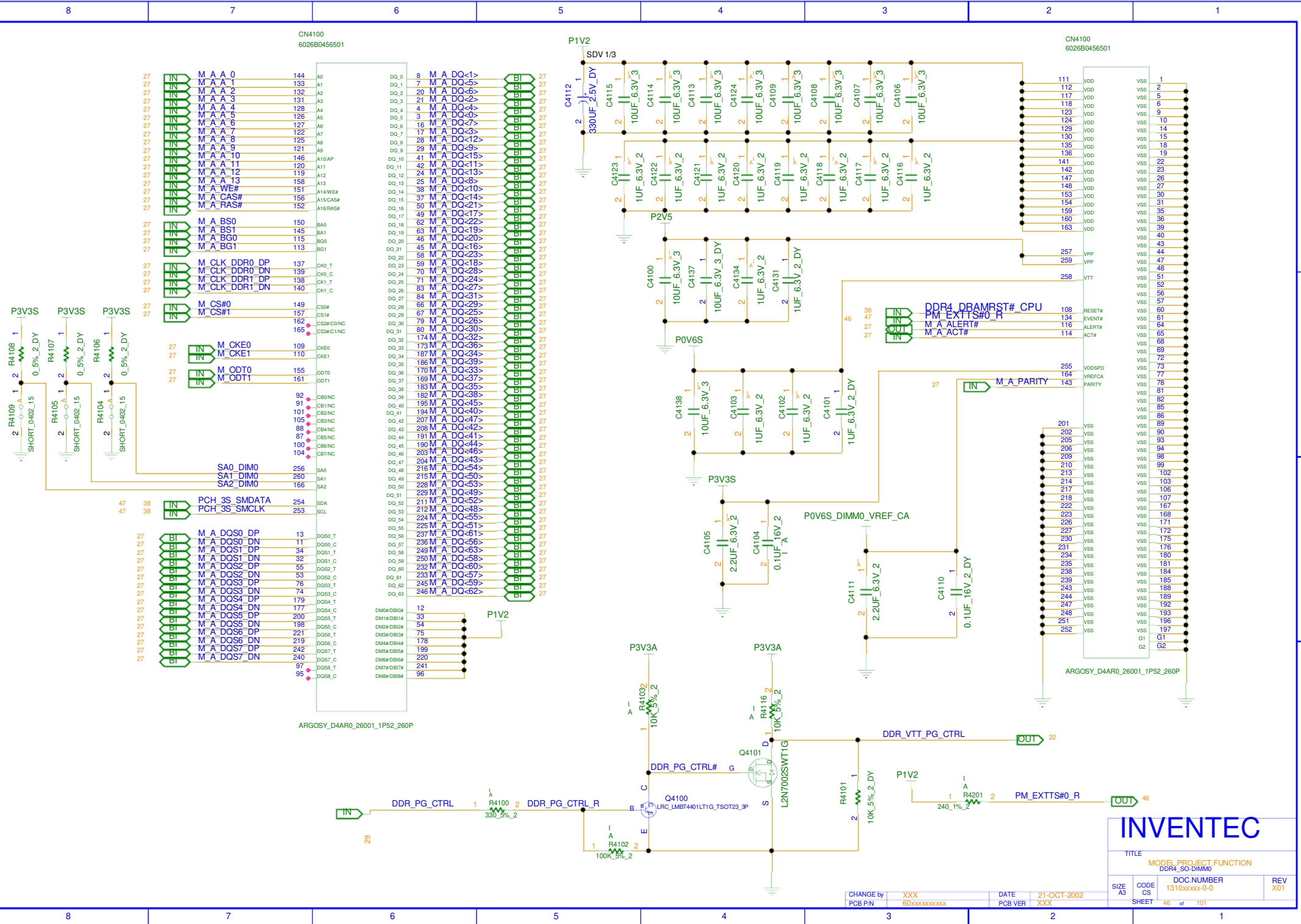


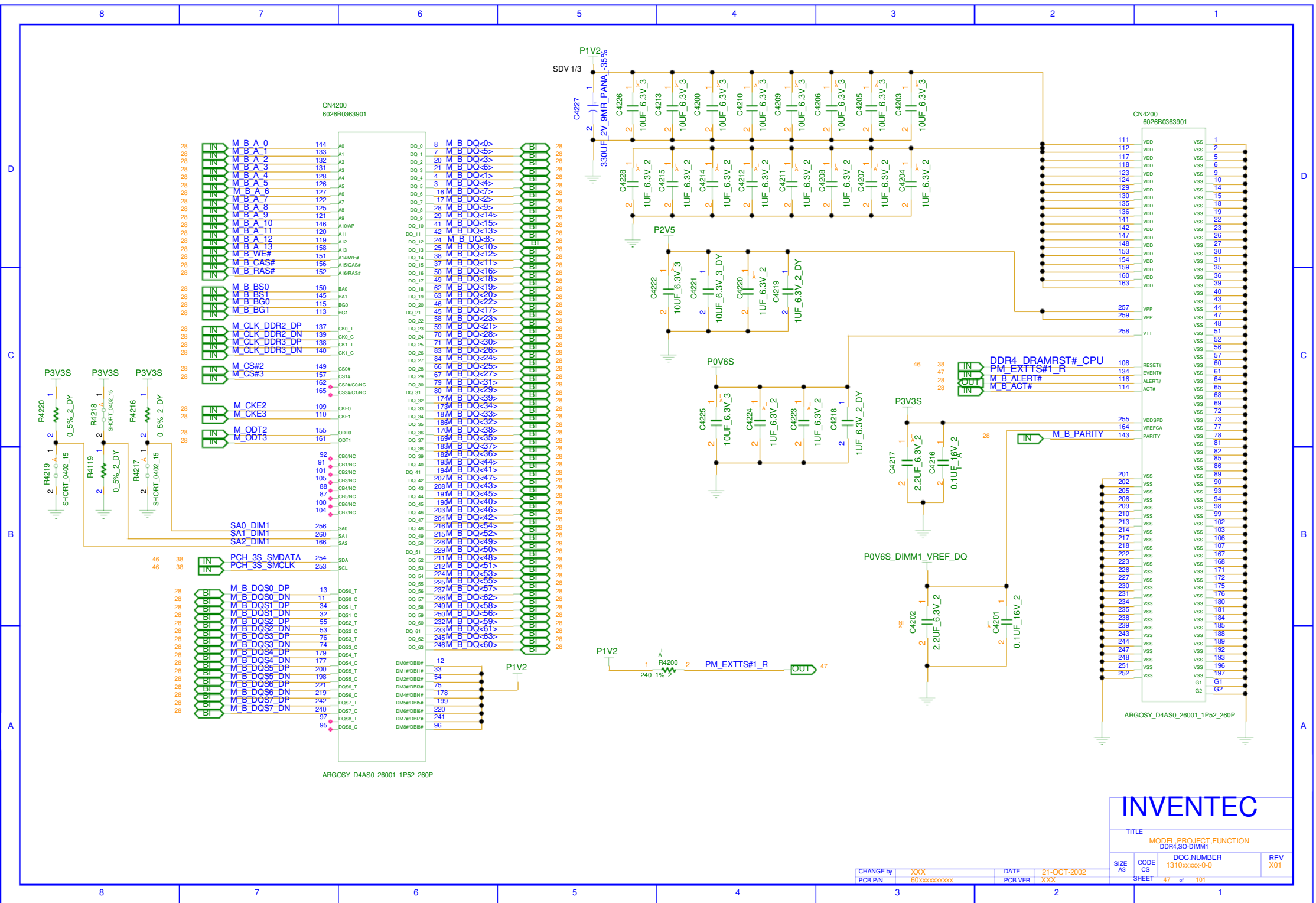


# INVENTEC

TITLE			MODEL,PROJECT,FUNCTION		
			Block Diagram		
SIZE	CODE	DOC. NUMBER			
A3	CS	1310xxxx-0-0			
SHEET		45	of	101	

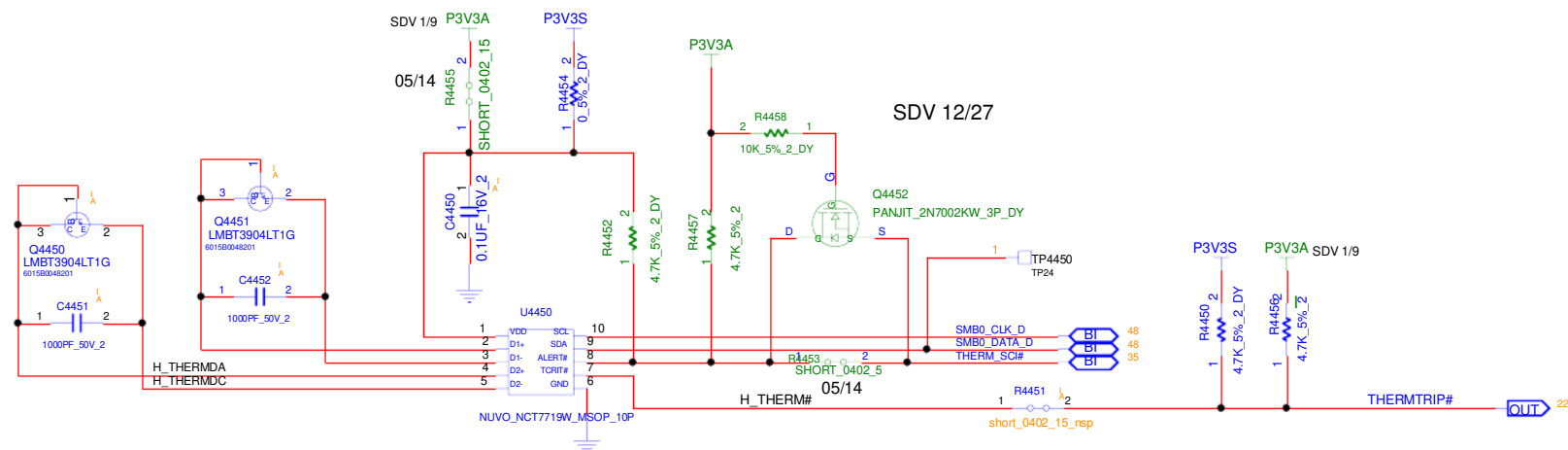
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX



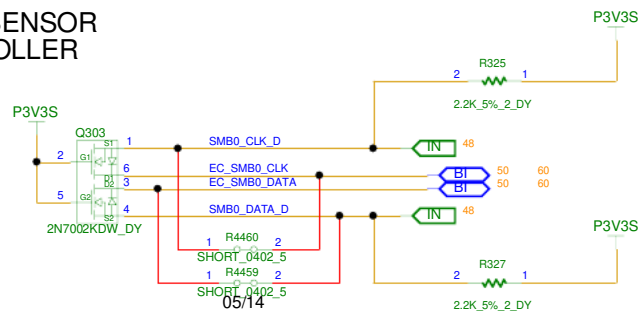


REFERENCE NUMBER:4450~4499

## THERM SENSOR

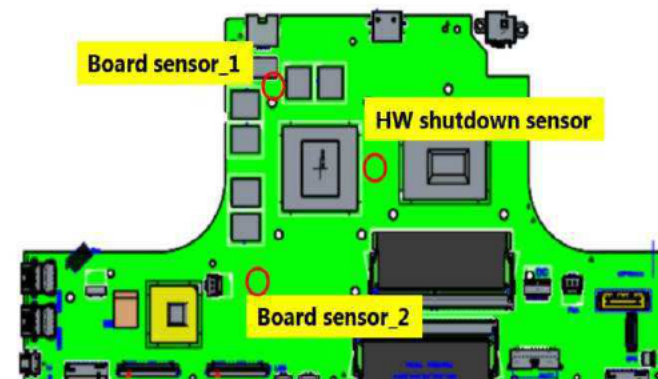
THERMAL SENSOR  
CC CONTROLLER

SDV 1/2



## BOARD SENSOR

- Board sensor\_1 monitor VRAM.
- Board sensor\_2 monitor GPU & VRAM power.



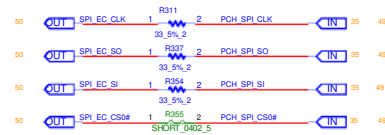
INVENTEC

TITLE  
MODEL PROJECT FUNCTION  
Block Diagram

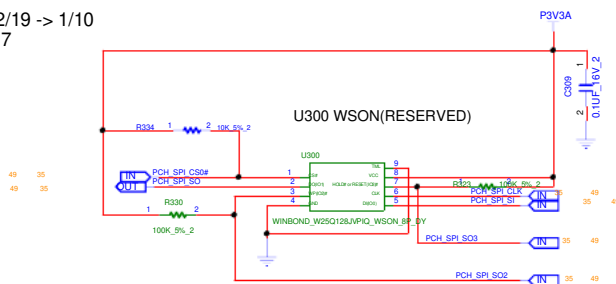
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01
SHEET		48 of 101	

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxx	PCB VER	XXX

REFERENCE 300~389(KBC)

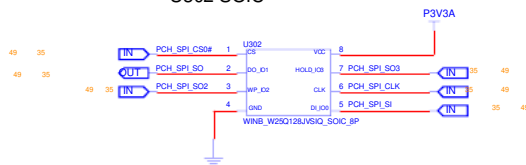


SDV 12/19 -> 1/10  
SIT 3/17

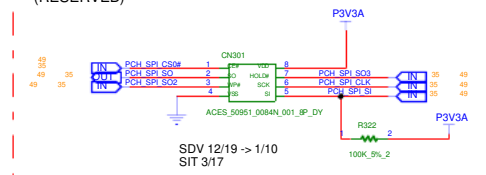


R330, R323 CLOSE TO PCH  
ALL EC & PCH RESISTOR NEED TO WITHIN 0.5" OF ROM (U300)

U302 SOIC



ROM SOCKET  
(RESERVED)



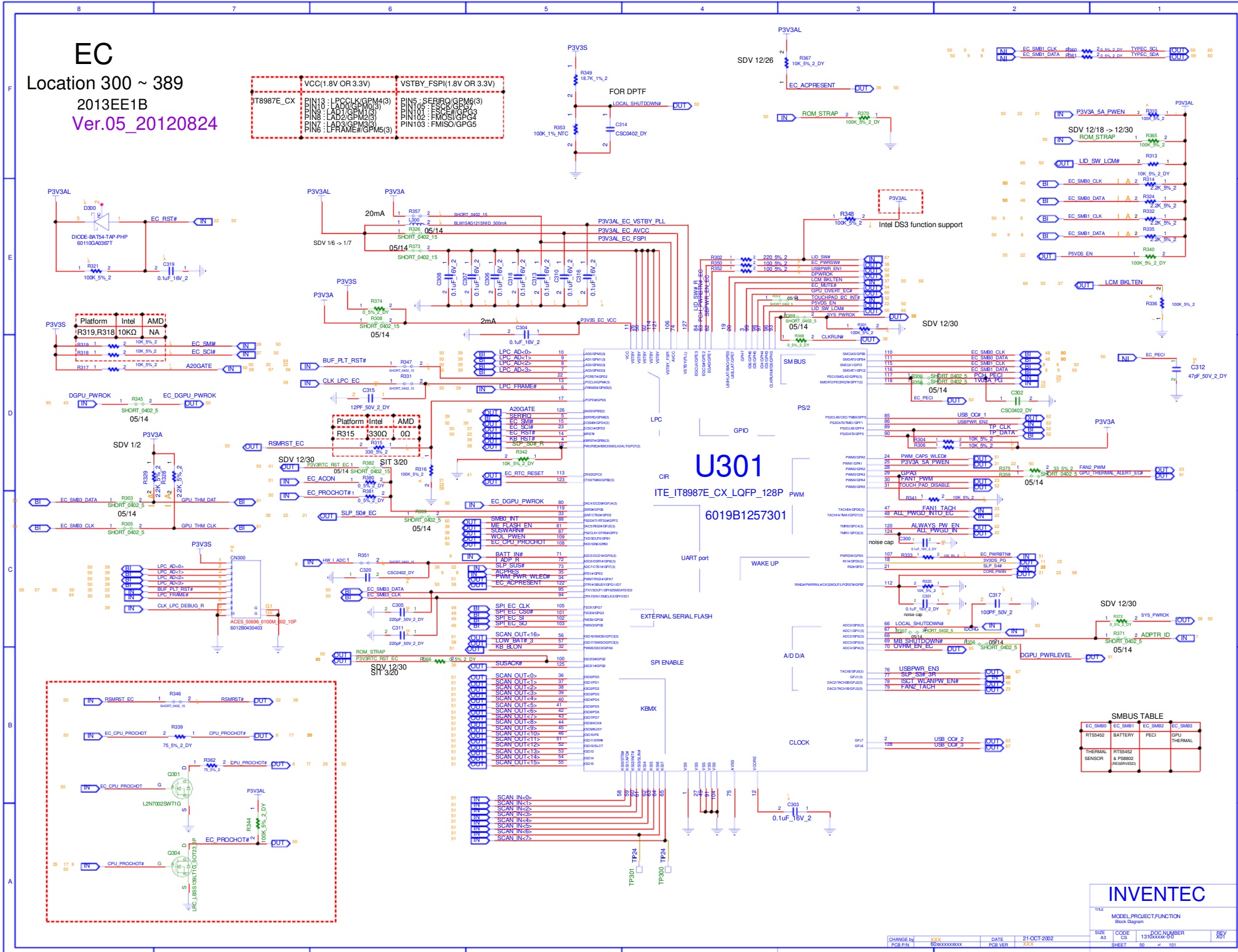
SDV 12/19 -> 1/10  
SIT 3/17

INVENTEC

TITLE			
MODEL PROJECT FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	131050000-01	001
SHEET	46	of 101	

CHANGED BY	XXX	DATE	21-OCT-2002
PCB P/N	W25Q128VPIQ	PCB VER	XXX

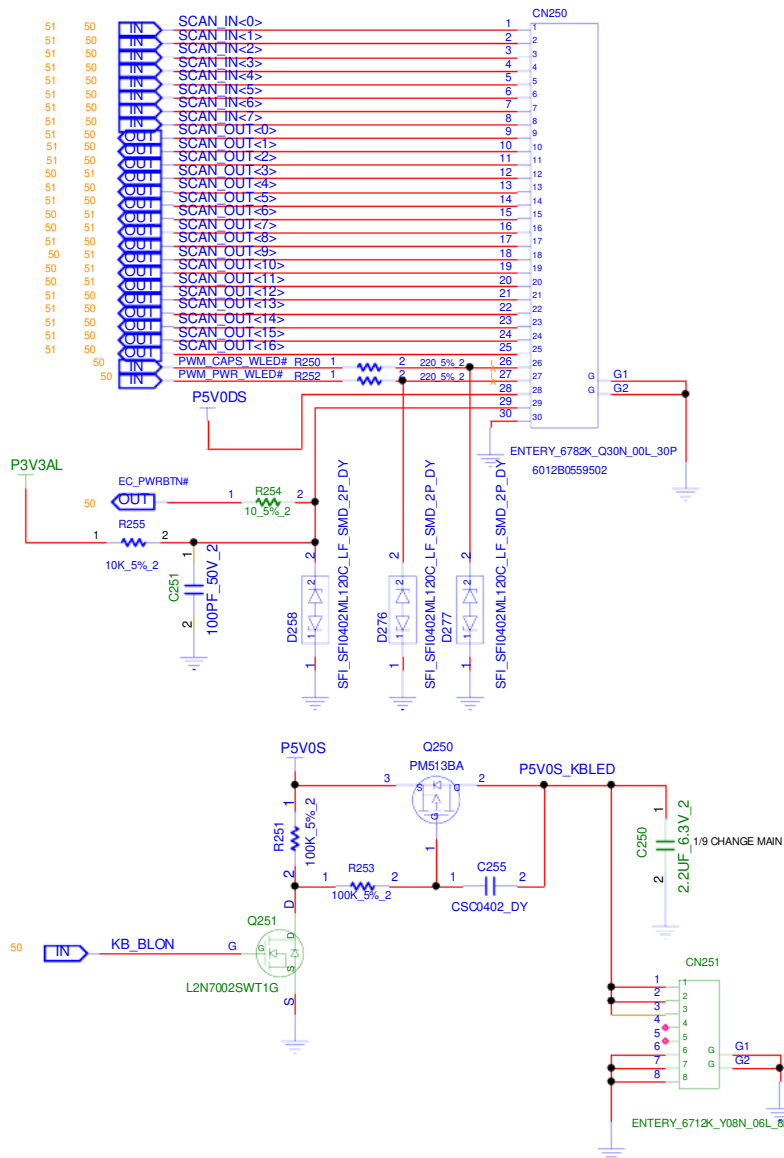
EC  
Location 300 ~ 389  
2013EE1B  
Ver.05 20120824



REFERENCE 200~249(POWER CONN)  
REFERENCE 250~299(KB/TP CONN)

## KEYBOARD CONN

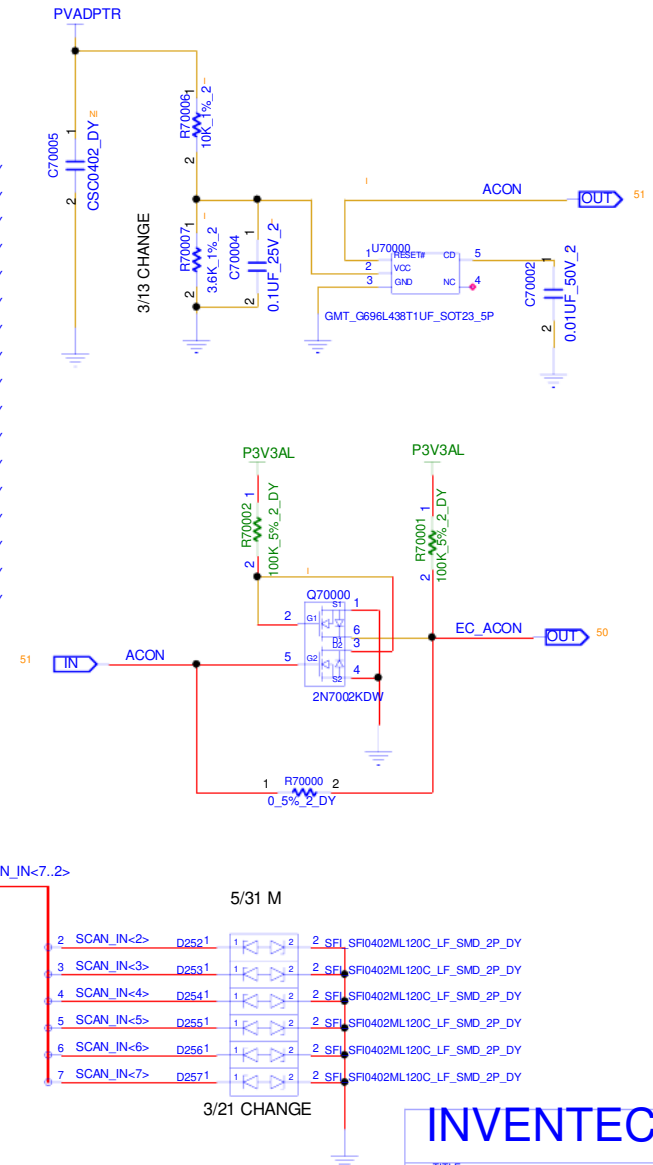
## RESERVED ADP-IN



## KB BACK LIGHT CONN

VCC : +5V  
LED V : 2.9~3.5V

	Min(LED V : 3.5V)	Max(LED V : 2.9V)
Power consumption	228.71mA	320.2mA

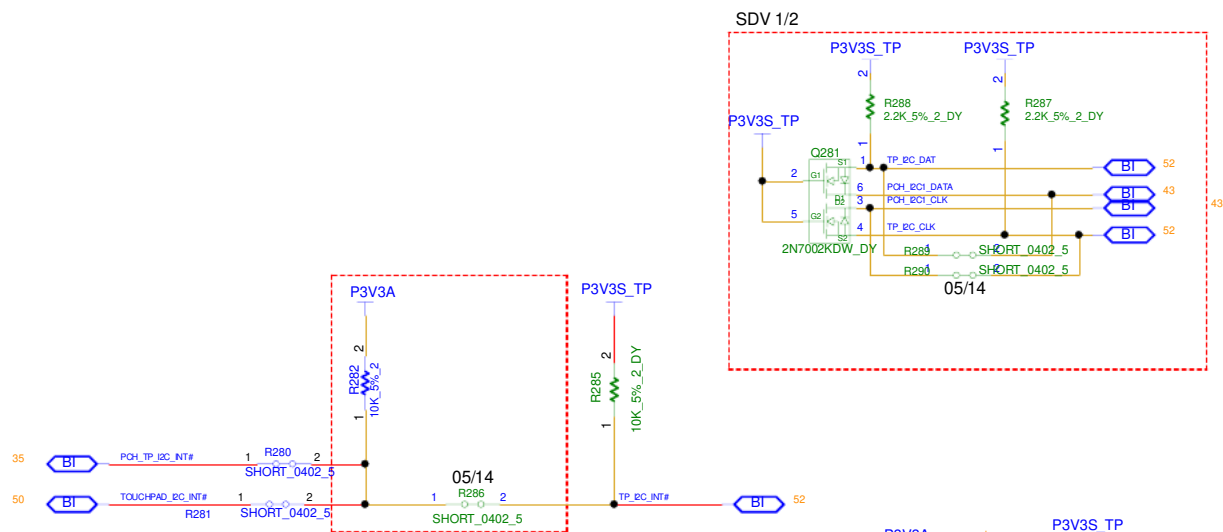


INVENTEC

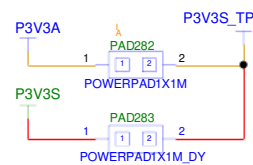
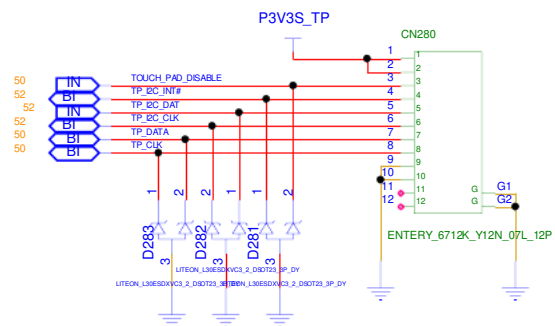
TITLE			
MODEL PROJECT FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET	51	of 101	

CHANGE by XXXX  
PCB P/N 60xxxxxxxxxx  
DATE 21-OCT-2002  
PCB VER XXXX





## TOUCHPAD CONN (CLICK PAD)



# INVENTEC

TITLE	MODEL,PROJECT,FUNCTION
	Block Diagram

SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET		52 of 101	

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX



	8	7	6	5	4	3	2	1
D								
C								
B								
A								
	8	7	6	5	4	3	2	1

INVENTEC

TITLE

MODEL PROJECT,FUNCTION  
Block Diagram

SIZE  
A3

CODE  
CS

DOC.NUMBER  
1310xxxxx-0-0

REV

X01

CHANGE by  
PCB P/N

XXX  
60xxxxxxxxxx

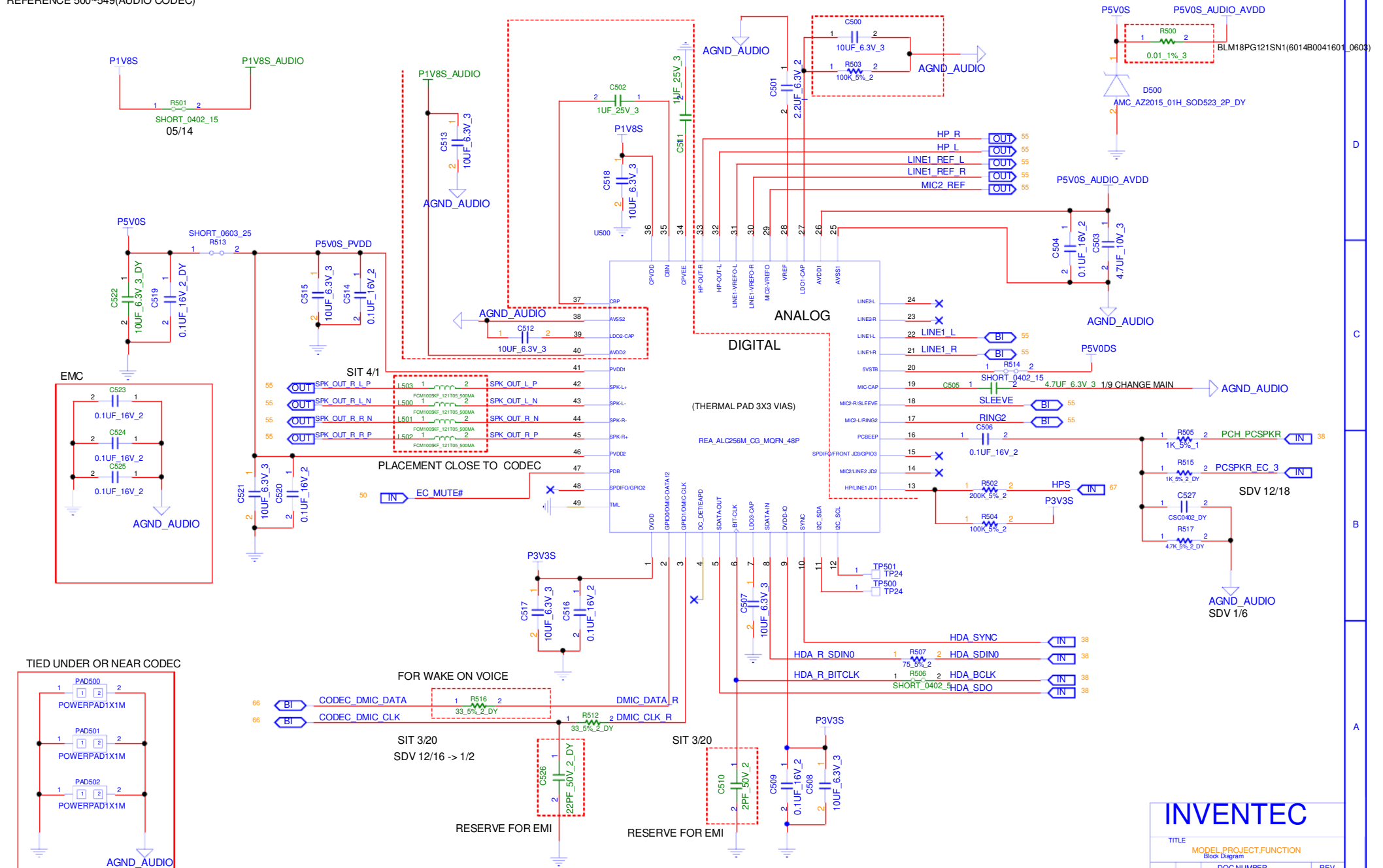
DATE  
PCB VER

21-OCT-2002  
XXX

SHEET

53 of 101

REFERENCE 500~549(AUDIO CODEC)



INVENTEC

TITLE  
MODEL PROJECT FUNCTION  
Block DiagramSIZE A3  
CODE CS  
DOC NUMBER  
1310xxxx-0-0  
REV  
X01

SHEET 54 of 101

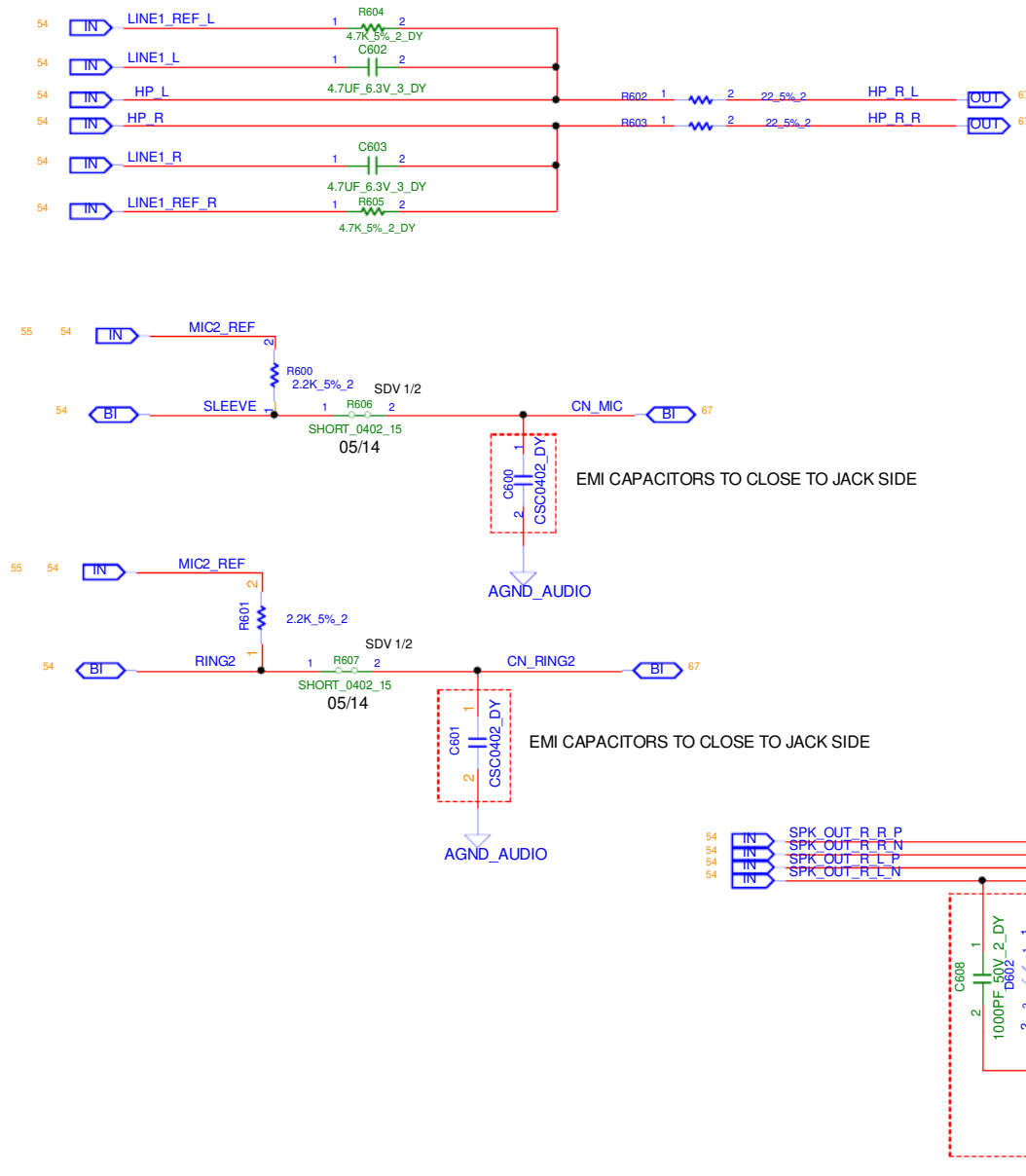
CHANGE by XXX  
PCB PN 60xxxxxxx  
DATE 21-OCT-2002  
PCB VER XXX

REFERCE 600~649(JACK/MIC/SPEAKER)

## AUDIO SPEAKER

CODEC SIDE

AUDIO CONNECTOR



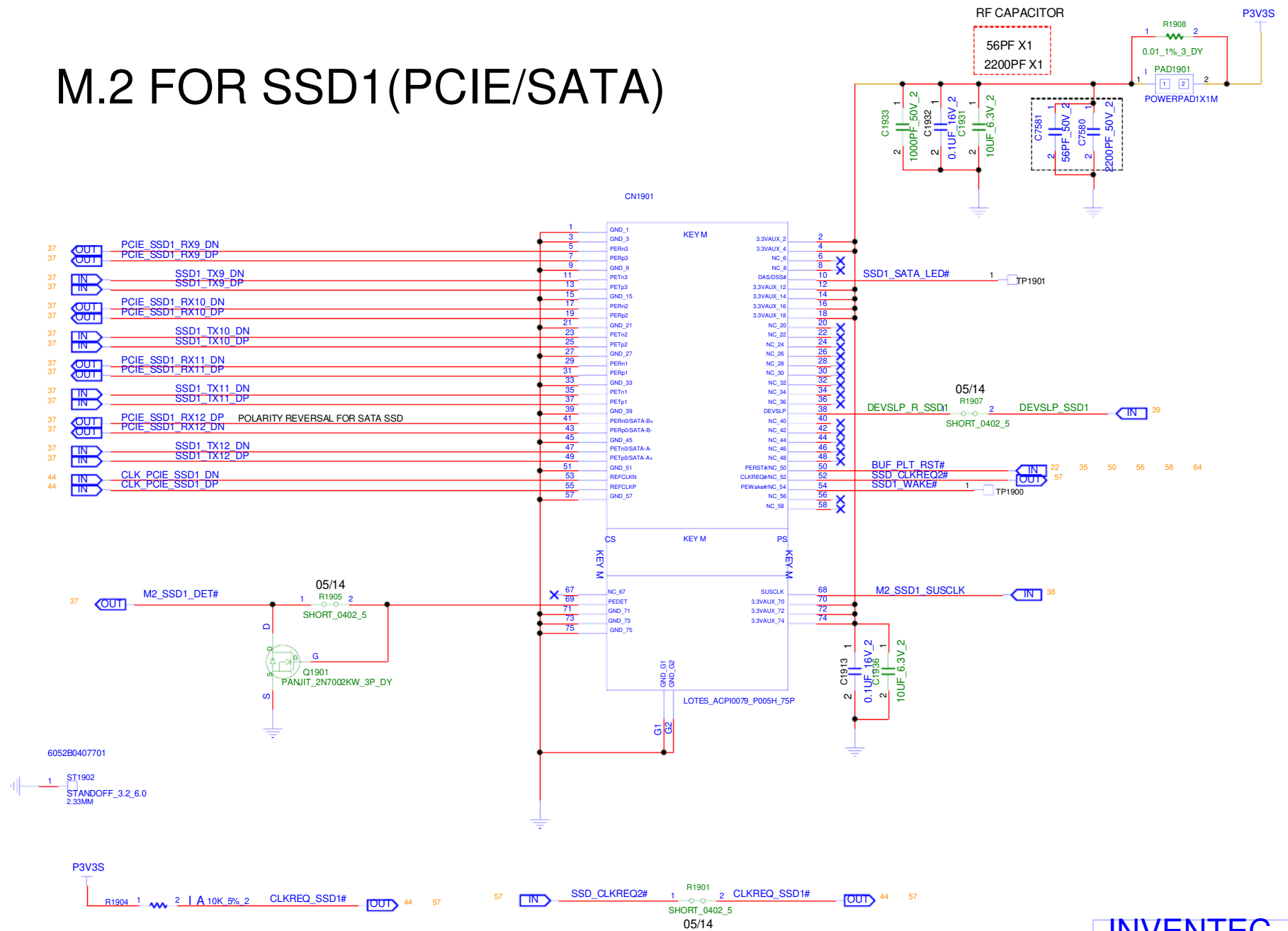
INVENTEC

TITLE			
Block Diagram			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET	55	of 101	

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxx	PCB VER	XXX



# M.2 FOR SSD1(PCIE/SATA)

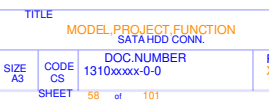


## INVENTEC

TITLE				
MODEL PROJECT FUNCTION				
Block Diagram				
SIZE	CODE	DOC NUMBER	REV	
A3	CS	1310xxxx-0-0	X01	
SHEET	57	of 101		

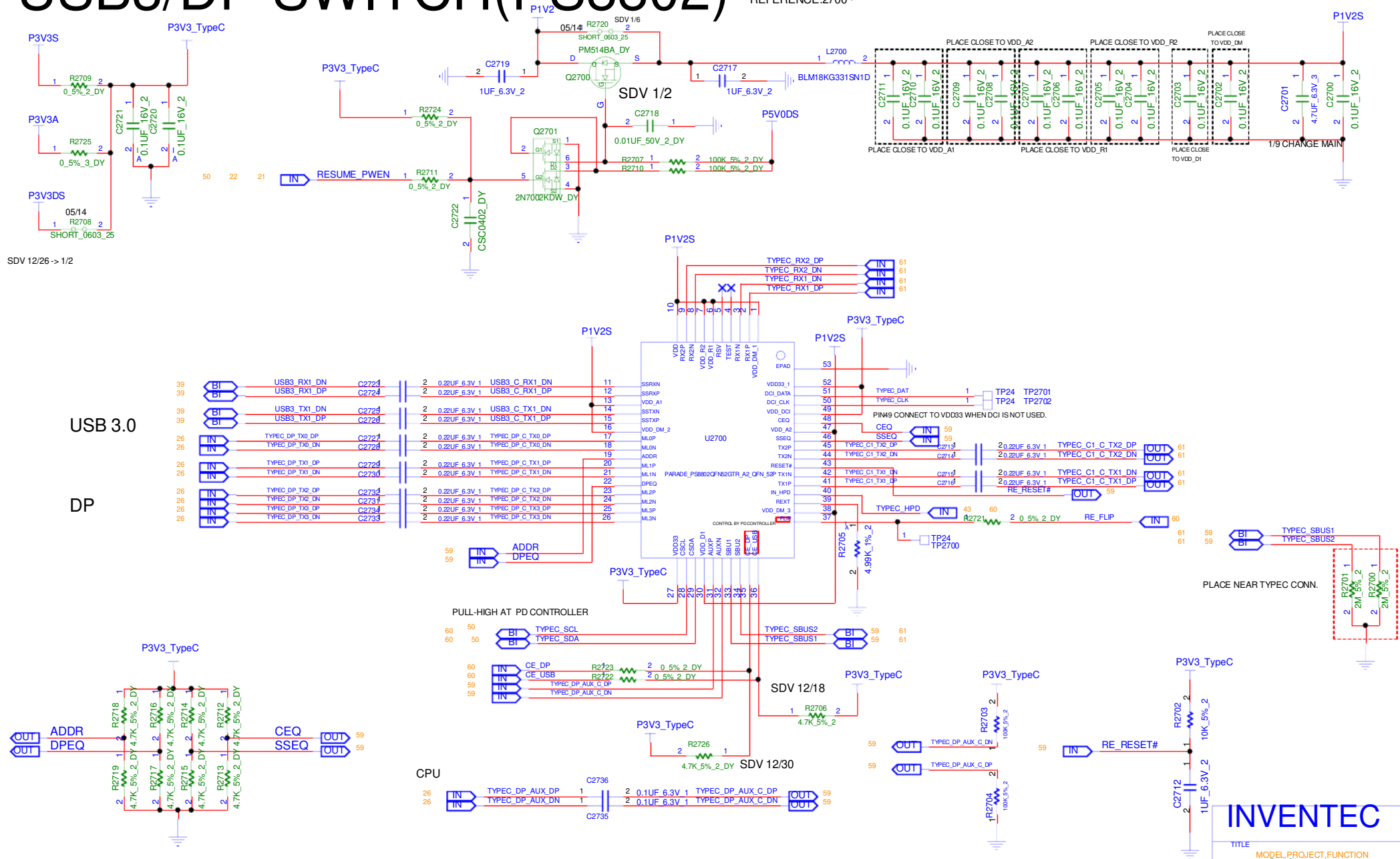
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxx	PCB VER	XXX

# INVENTEC

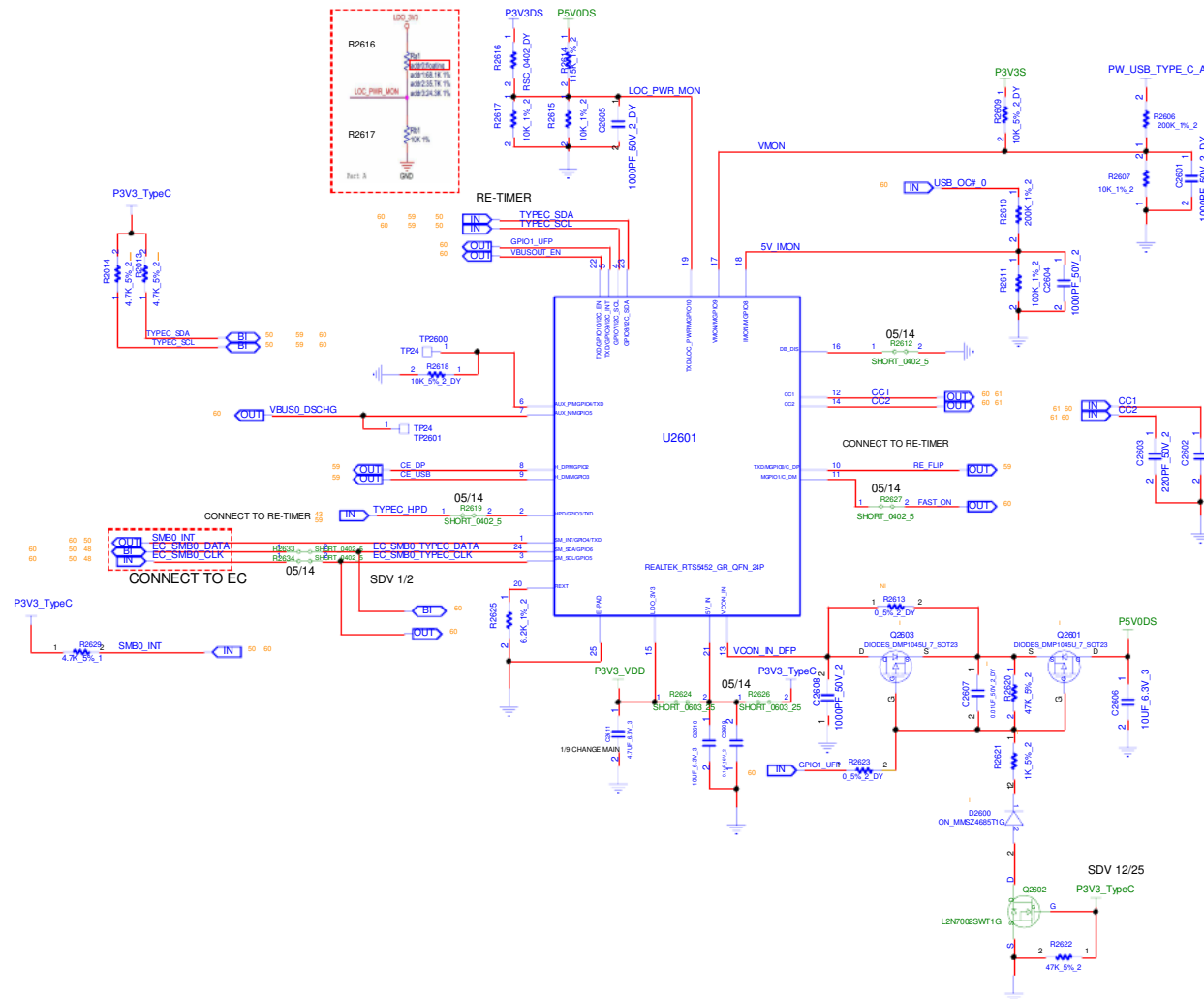
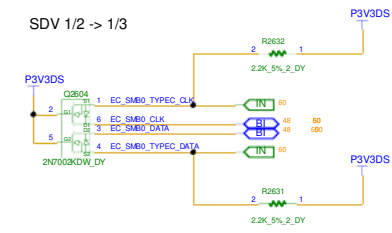
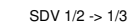
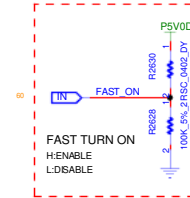
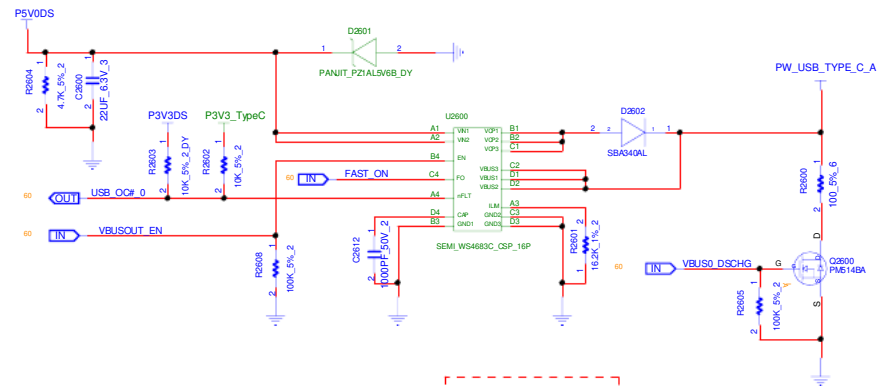


## USB3/DP SWITCH(P58802)

REFERENCE:2700~



# CC-CONTROLLER(RTS5452)

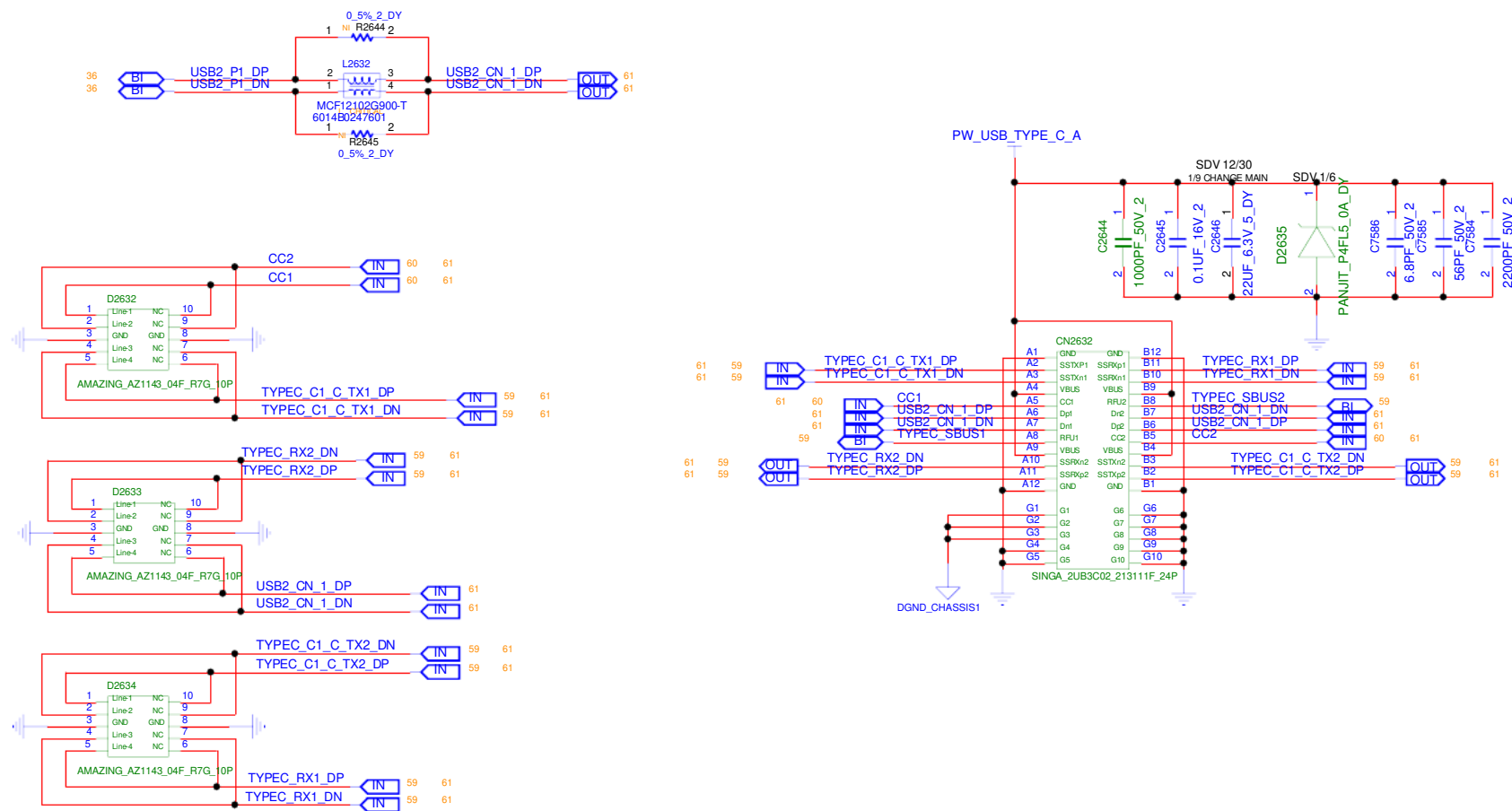


INVENTEC				
TITLE				
MODEL_PROJECT/FUNCTION				
TPS5450				
SIZE C	CODE CS	DOC NUMBER 1310XXXX-00		REV X01
SHEET		of	50	101

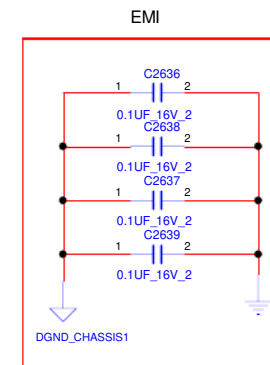
CHANGE by	XXX	DATE	21-OCT-2002	SIZE	C	CODE	CS	DOC NUMBER	1310XXXX-00	REV	X01
PCB PIN	606000000000	PCB VER	XXX <VR>	SHEET of 60 101							



TYPE-C CONN.



56PF X1    6.8PF X1  
2200PF X1



# INVENTEC

TITLE			
MODEL PROJECT FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
SHEET 61 of 101			

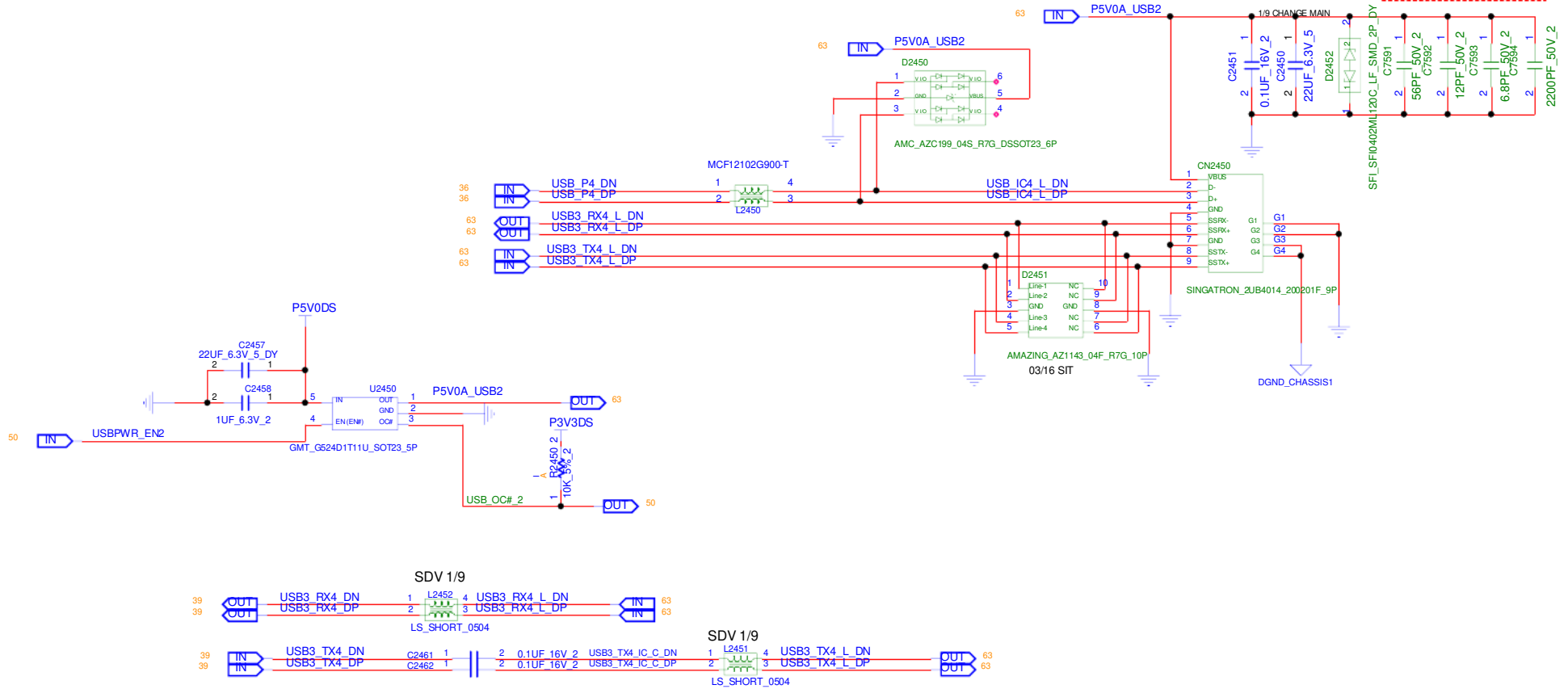


REFERENCE 2450~2599(USB3.0)

## USB 3.0 PORT2

RF CAPACITOR

56PF X1	6.8PF X1
12PF X1	2200PF X1



INVENTEC

TITLE

MODEL PROJECT FUNCTION

Block Diagram

SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET	63	of 101	

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxx	PCB VER	XXX

# LAN (Controller)

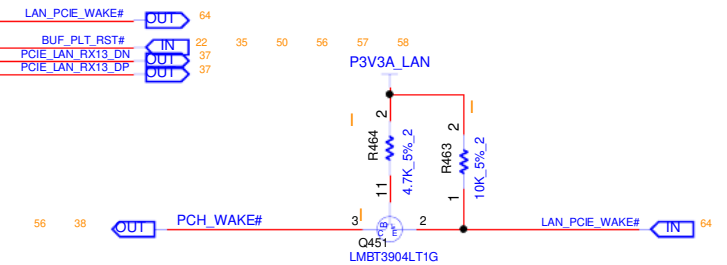
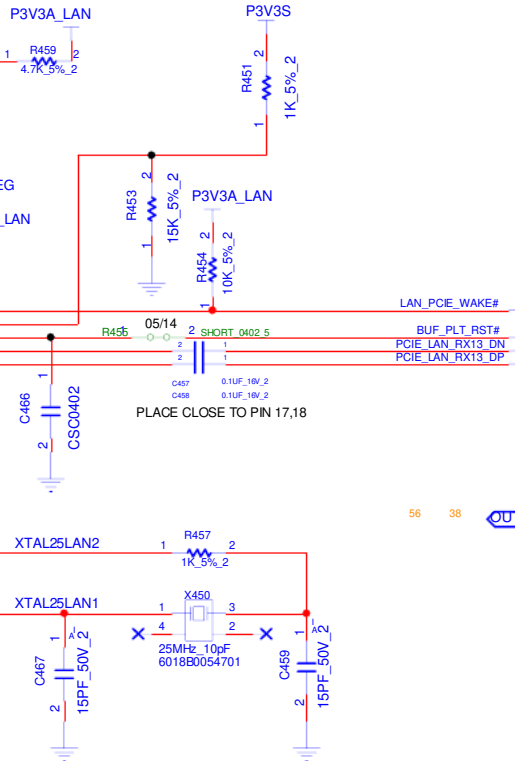
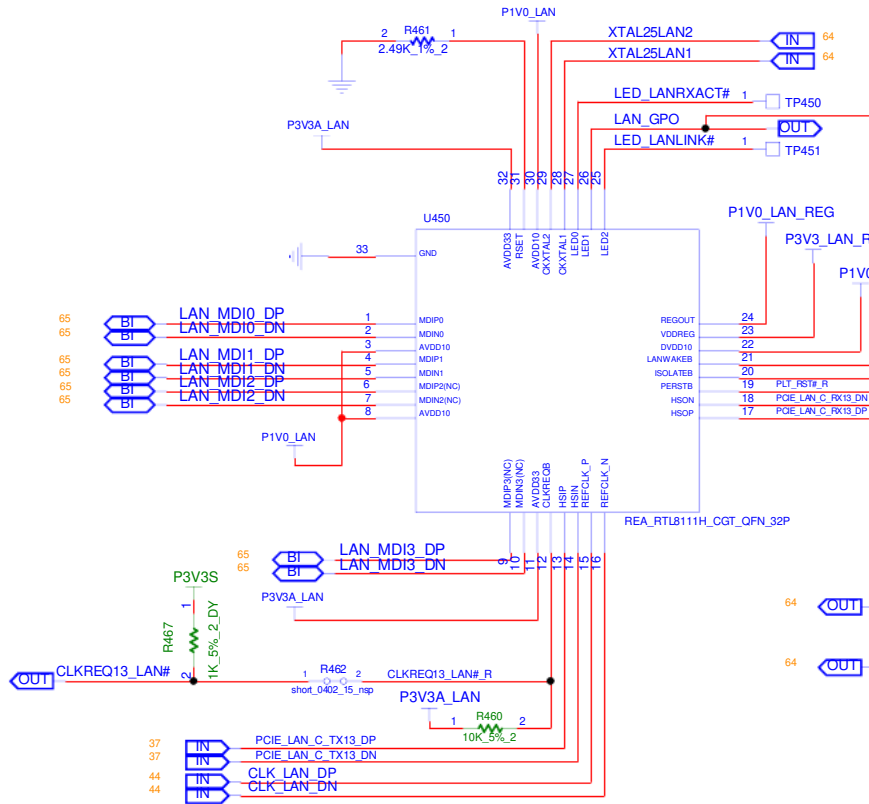
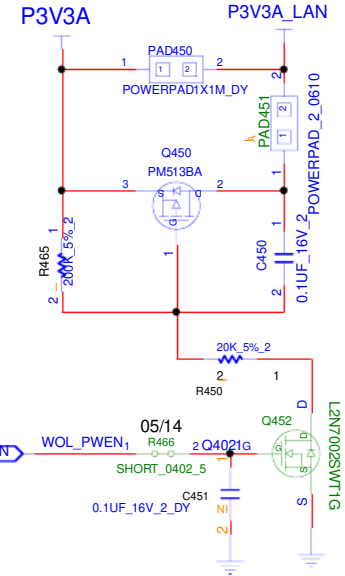
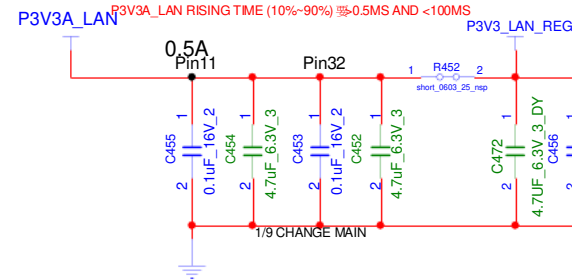
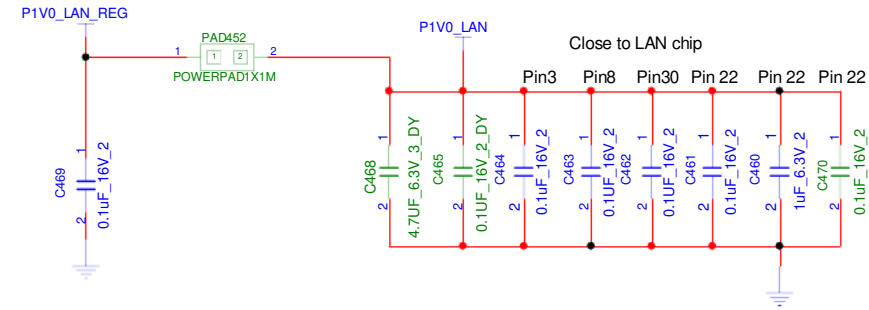
LOCATION 450 ~ 499

Ver.03\_210120807

01. 請註記 +3V\_LAN Rising time (10%~90%)要&gt;0.5mS and &lt;100mS.

02. LAN power Noise +3V\_LAN &lt; 200mV Vpeak to Vpeak.

03. LAN power Noise P1V0\_LAN &lt; 100mV Vpeak to Vpeak.



INVENTEC

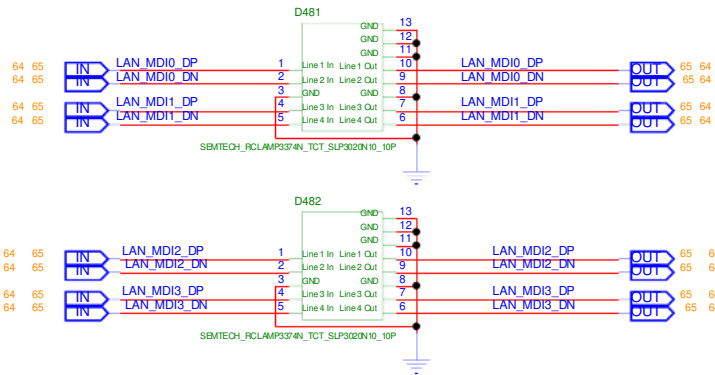
TITLE				
MODEL PROJECT.FUNCTION				
Block Diagram				
SIZE	CODE	DOC.NUMBER	REV	
A3	CS	1310xxxx-0-0	X01	
SHEET	64	of 101		

CHANGE by XXX  
PCB P/N 60xxxxxxxxDATE 21-OCT-2002  
PCB VER XXX

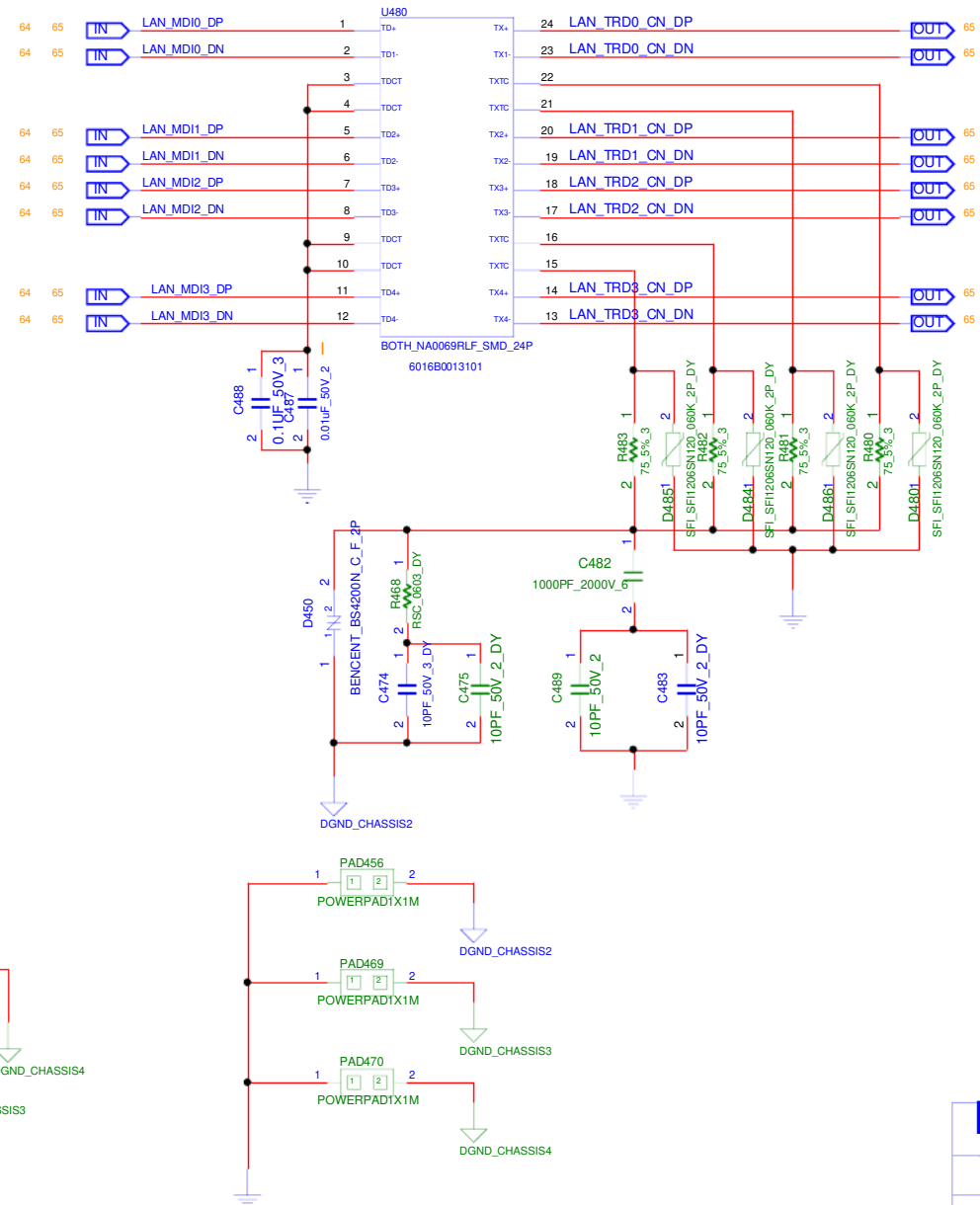
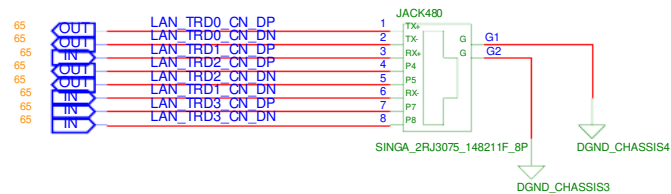
REFERENCE 450~499

## TRANSFORMER

## ESD



## RJ-45



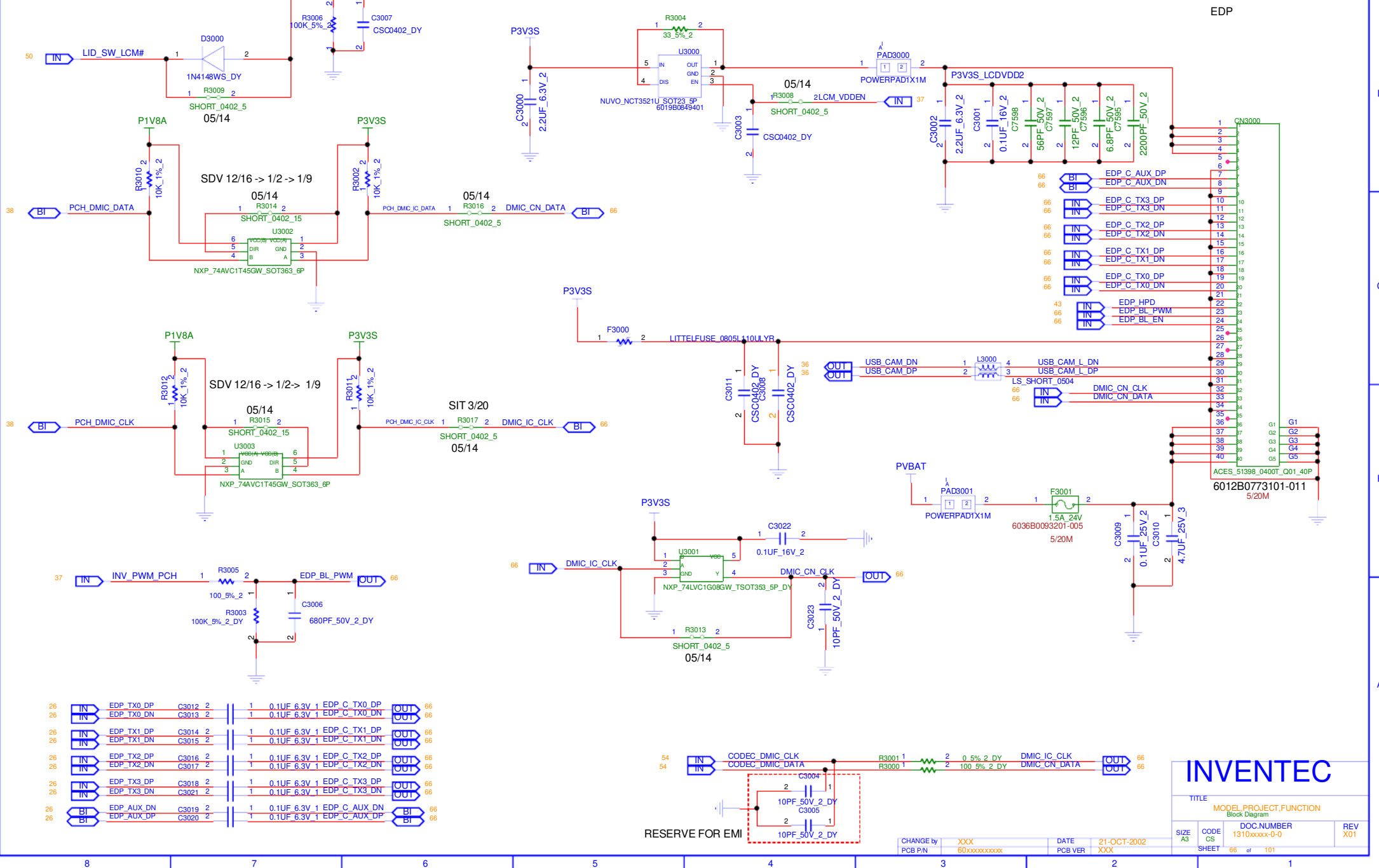
INVENTEC

TITLE			
MODEL PROJECT.FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET	65	of 101	

CHANGE by XXXX DATE 21-OCT-2002  
PCB P/N 60xxxxxxx PCB VER XXXX

REFERENCE 3000~3049(LCM)

# EDP CONN

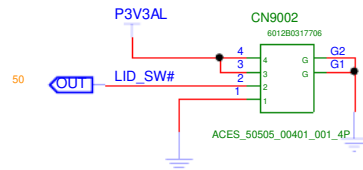


# INVENTEC

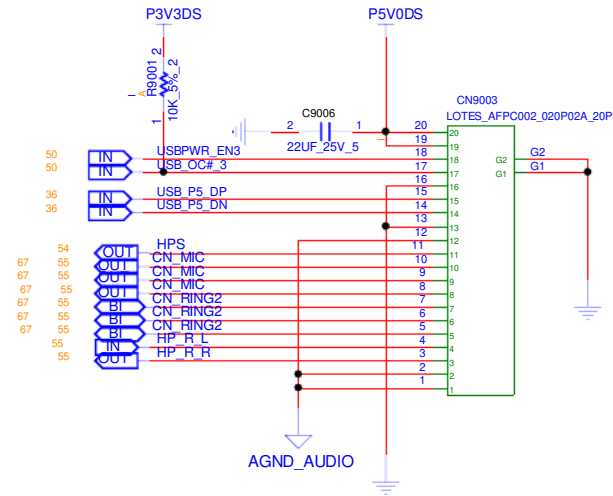
TITLE	MODEL, PROJECT, FUNCTION
	Block Diagram

SIZE A3	CODE CS	DOC.NUMBER 1310xxxx-0-0	REV X01
SHEET		66 of 101	

## HALL SENSOR BOARD CONN



## SMALL BOARD CONN

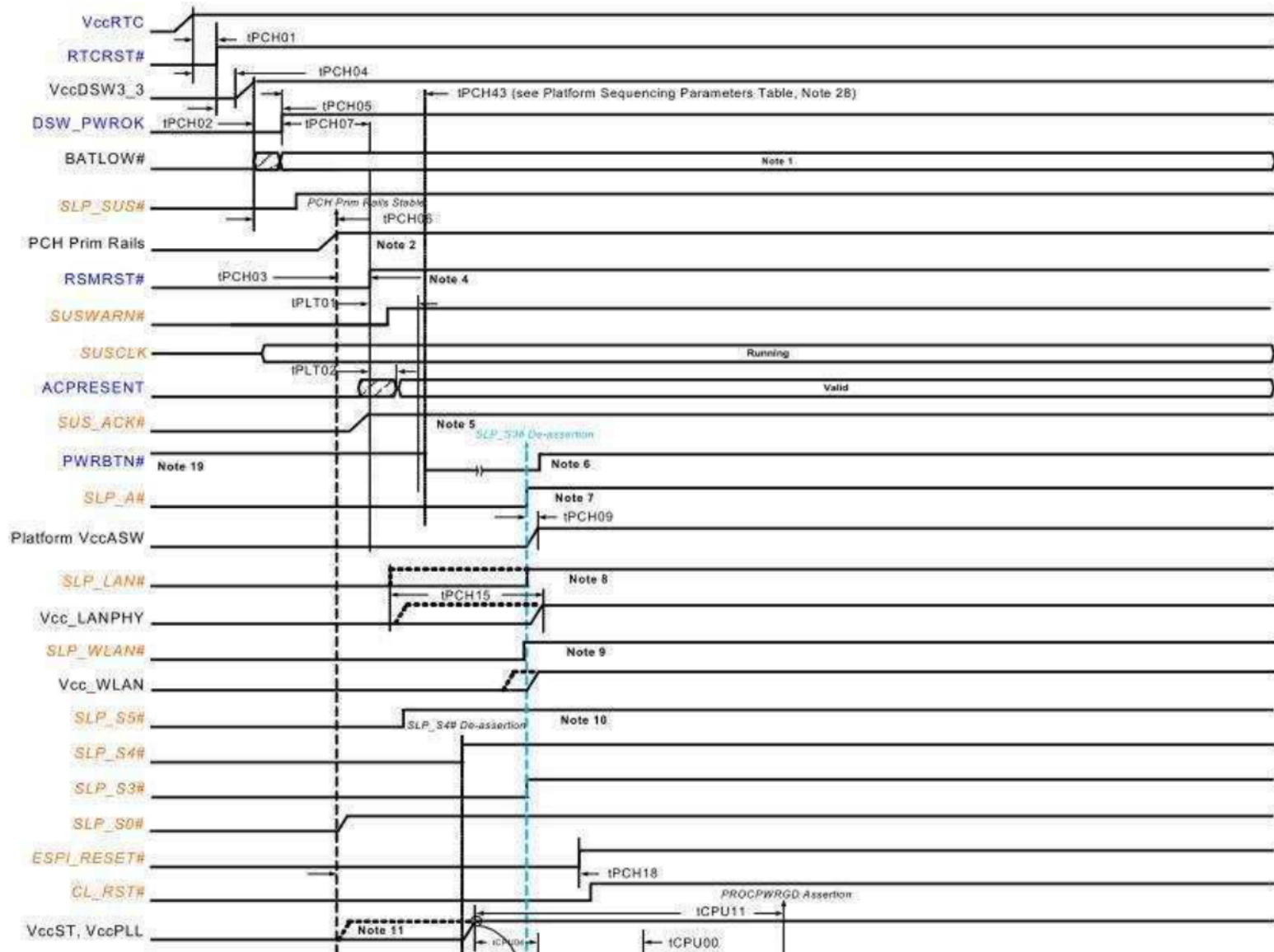


INVENTEC

TITLE  
MODEL PROJECT FUNCTION  
Block Diagram

SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
SHEET 67 of 101			

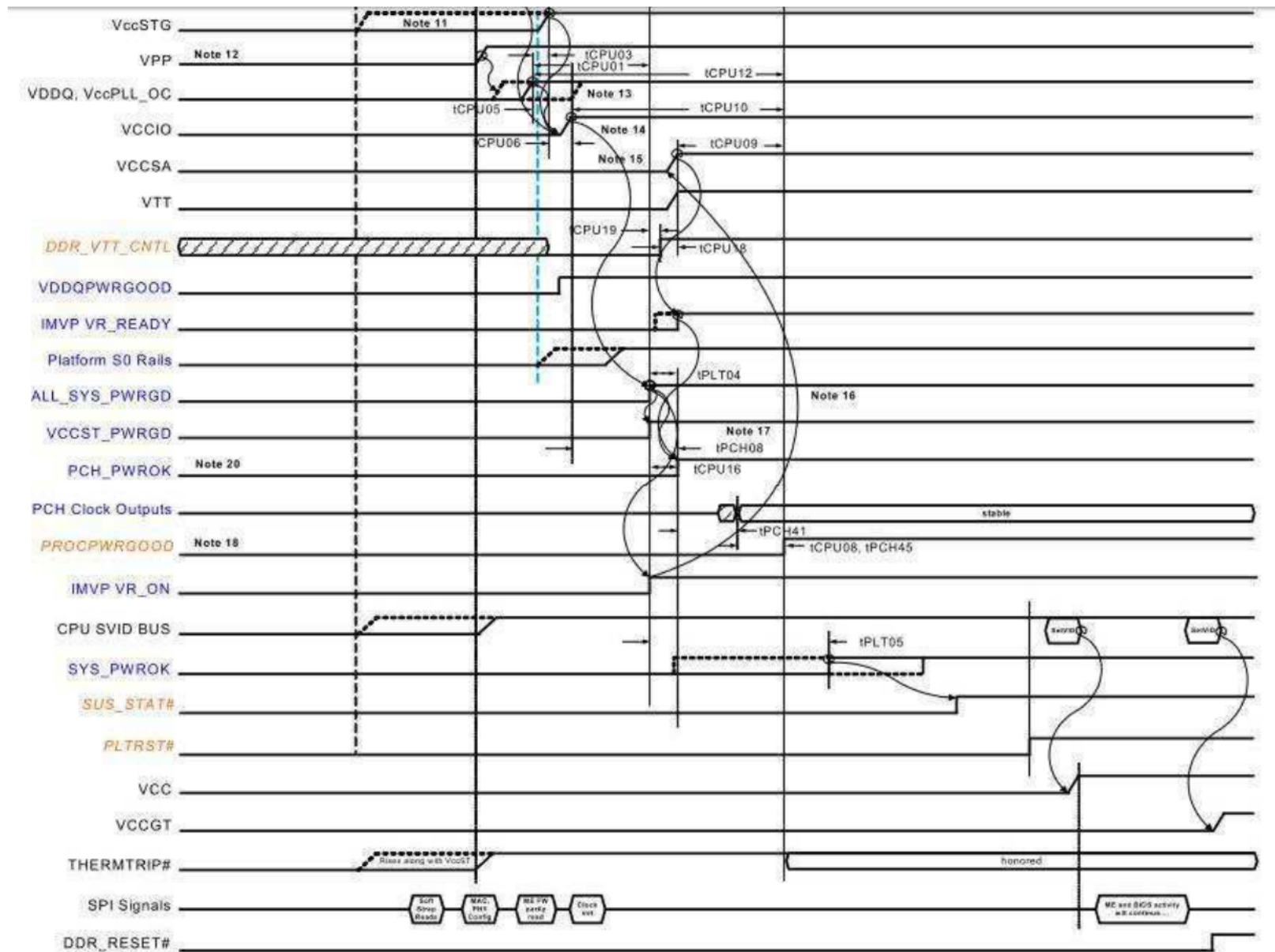
CHANGE by PCB P/N	XXX 60xxxxxxxx	DATE PCB VER	21-OCT-2002 XXX
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**INVENTEC**TITLE  
MODEL PROJECT FUNCTION  
Block Diagram

SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
SHEET 68 of 101			

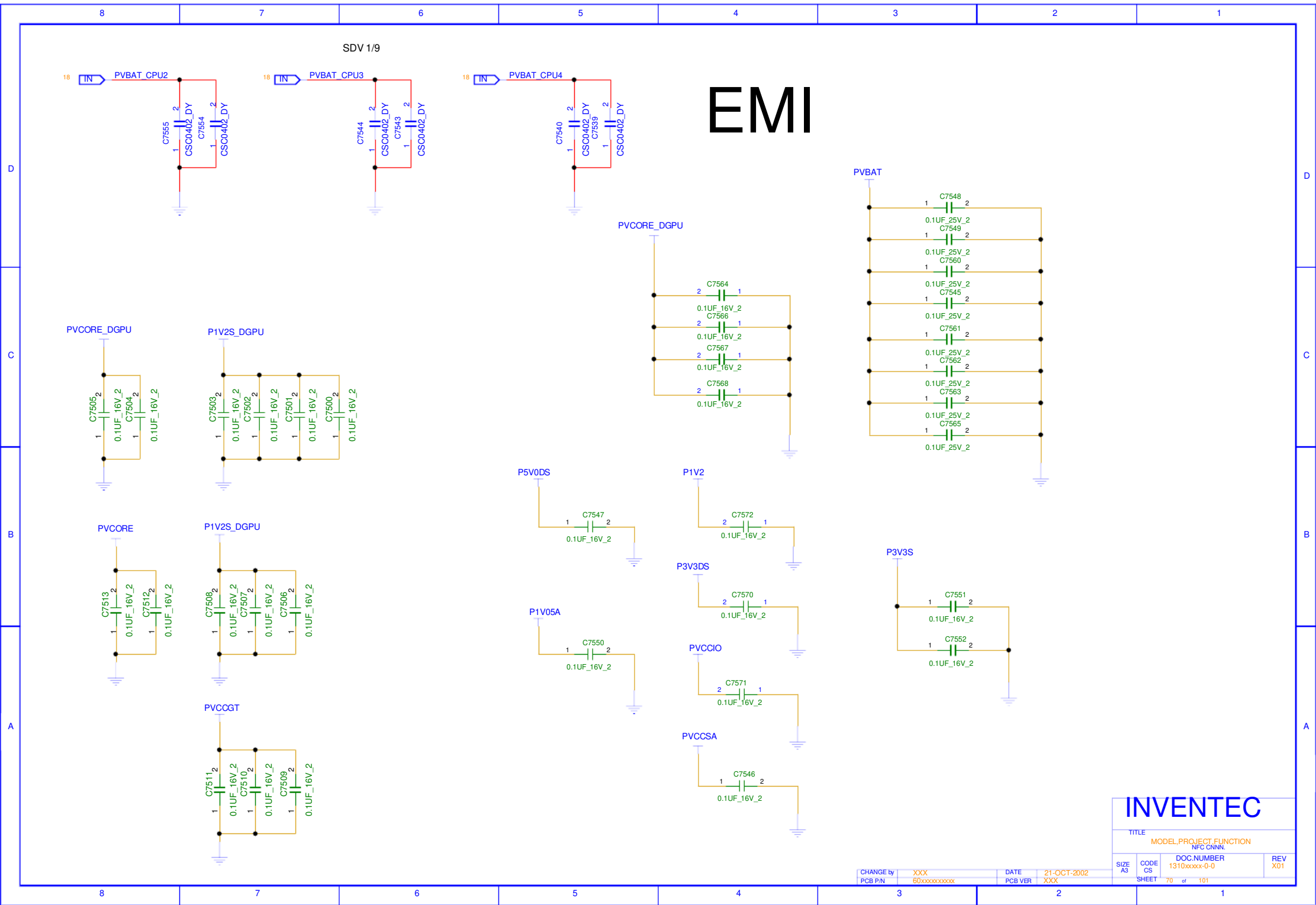
CHANGE by PCB P/N	XXX 60xxxxxxxx	DATE PCB VER	21-OCT-2002 XXX
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INVENTEC

TITLE			
MODEL PROJECT.FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	X01
SHEET	69	of 101	



INVENTEC

TITLE

MODEL PROJECT FUNCTION

NFC CANN

SIZE A3

CODE CS

DOC NUMBER 1310xxxx-0-0

REV X01

SHEET 70 of 101

87654321

D

D

C

C

B

B

A

A

RESERVED

INVENTEC

TITLE			
MODEL PROJECT FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
SHEET	71	of	101

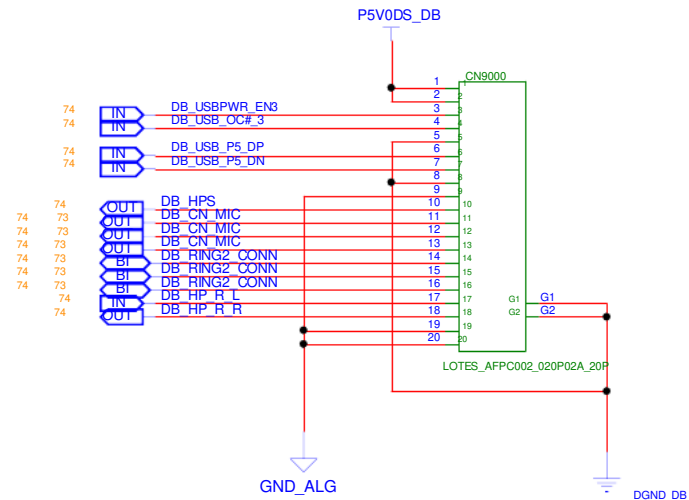
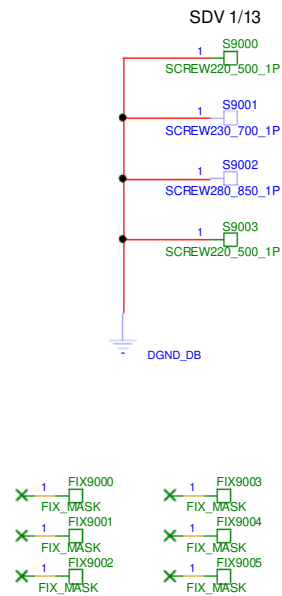
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxx	PCB VER	XXX

87654321

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SHEET		72	of		101



INVENTEC

TITLE  
MODEL PROJECT FUNCTION  
Block Diagram

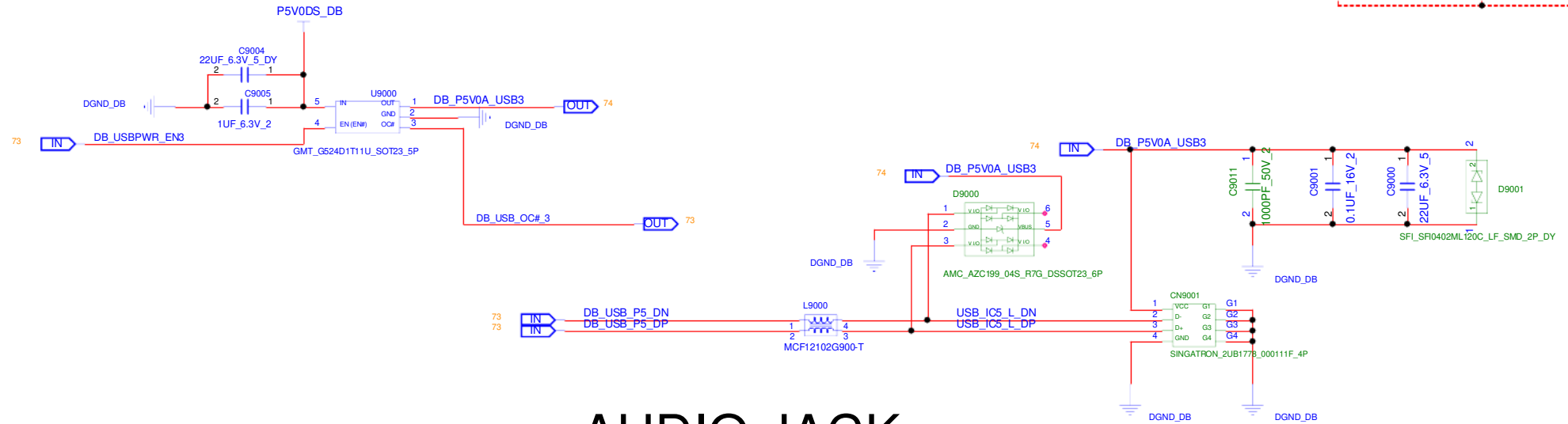
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SHEET 73 of 101			

CHANGE by PCB P/N	XXX 60xxxxxxxxxx	DATE PCB VER	21-OCT-2002 XXX
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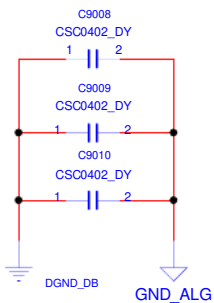
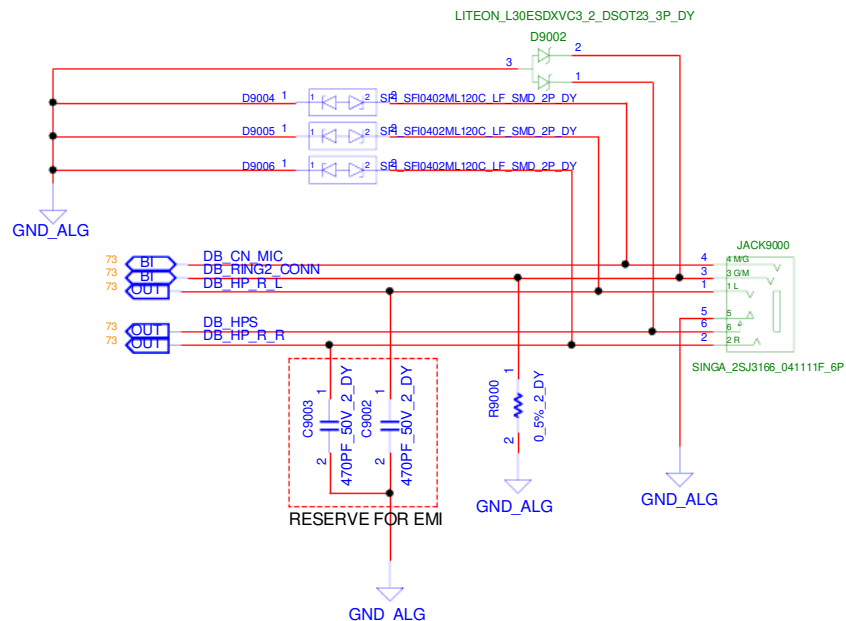
REFERENCE 9000~(USB2.0)

# USB2.0 CNTR

D2000	NOTE
6011B0158001 ->6011B0158201	ADD D2001



## AUDIO JACK

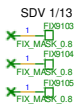


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MODEL PROJECT FUNCTION			
Block Diagram			
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SHEET	74	of 101	

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxx	PCB VER	XXX

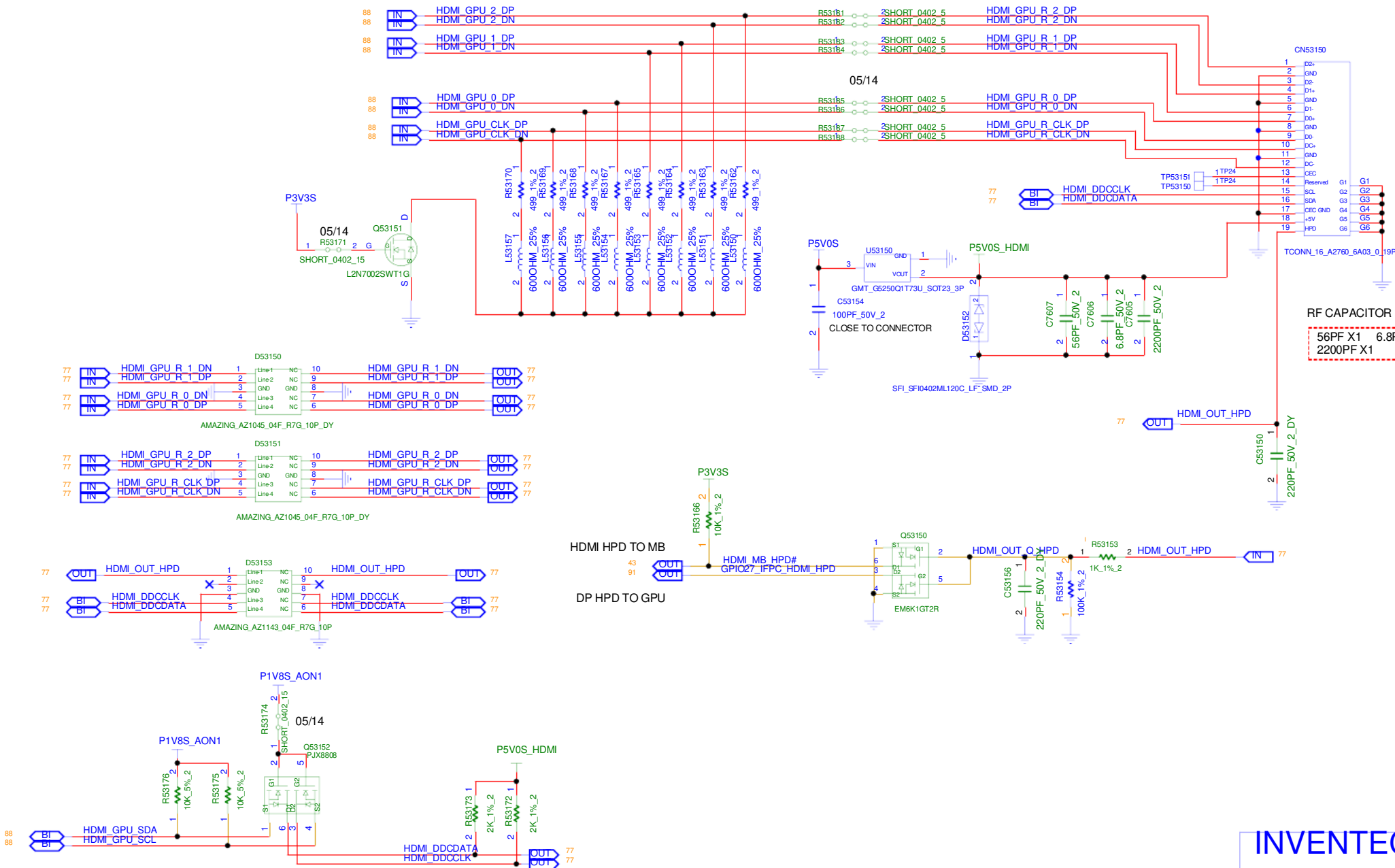
A	
B	
C	
D	
E	
F	



RESERVED

INVENTEC





# INVENTEC

TITLE			
MODEL PROJECT,FUNCTION			
Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxx-0-0	REV X01
SHEET		77 of 101	



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxx	PCB VER	XXX

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NOTES:  
1. HSF Property: Comply iSupplier system HSF property attribute up-to-date value.

N18P-G62

GDDR6 29X29(4PCS)

2020.1.13

21OCT-2002		
DATE	CHANGE NO.	REV

DESIGN/ DRAWER	XXX	DATE	21OCT-2002
CHECK			
APPROVAL			
FILE NAME			
PCB P/N	02000XXXXX	PCB VER	XXX

INVENTEC			
TITLE MODEL PROJECT FUNCTION			
SIZE	CODE	DOC NUMBER	REV
3	GS	131000002-00	001
SHEET	of	75	101

SHEET	CONTENT	SHEET	CONTENT
79	COVER	94	POWER SEQUENCE MAP
80	GPU Index	95	POWER SEQUENCE
81	GPU PCI-E GEN3 X 16	96	POWER LOAD & DISCHARGER
82	GPU FRAME BUFFER A	97	GPU_NVVDD (MP2884A)
83	GPU MEMORY FBA PARTITION 31-0	98	PVCORE_DGPU (MP86941_1-2P)
84	GPU MEMORY FBA PARTITION 63-32	99	P1V2S_DGPU (RT8237)
85	GPU FRAME BUFFER B	100	P1V0S_DGPU (RT8068A)
86	GPU MEMORY FBB PARTITION 31-0	101	P1V8S_DGPU (RT8068A)
87	GPU MEMORY FBB PARTITION 63-32	102	
88	GPU HDMI/DP	103	
89	GPU LVDS	104	
90	GPU BIOS/EXTERNAL STRAPS	105	
91	GPU GPIOs	106	
92	GPU POWER/GND	107	
93	OVR-M	108	

**INVENTEC**TITLE  
MODEL PROJECT.FUNCTION  
Block Diagram

CHANGE by PCB P/N	XXX 60xxxxxxxxxx	DATE PCB VER	21-OCT-2002 XXX	SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
				SHEET	80	of	101





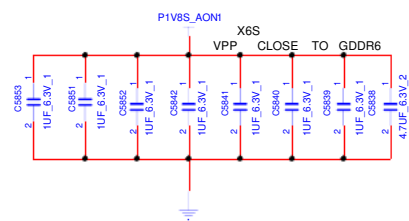
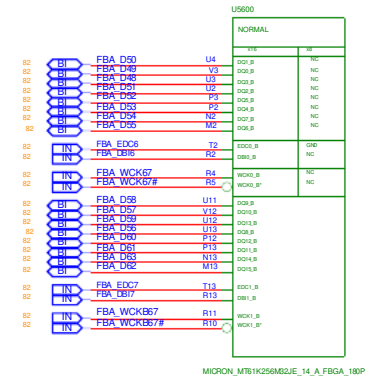
### M3



INVENTEC

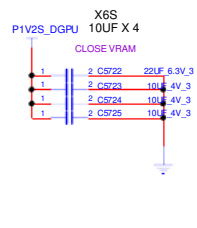
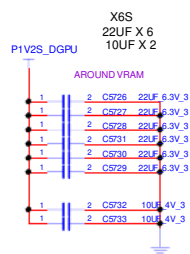
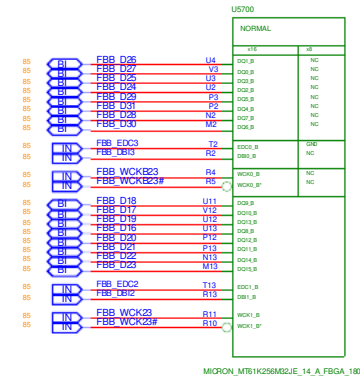
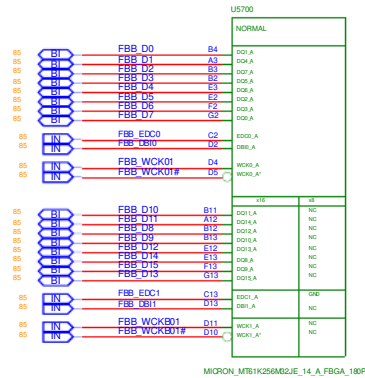
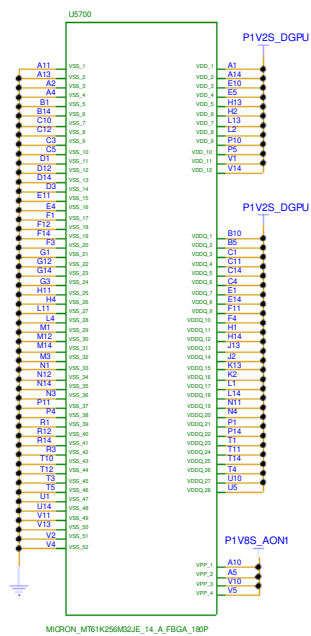
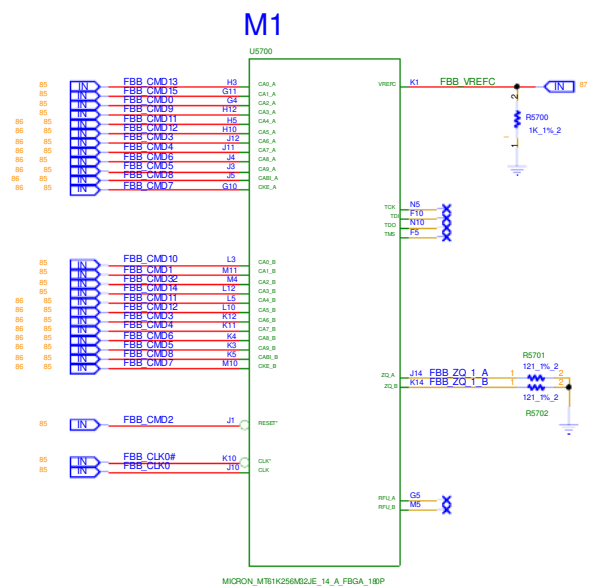


## M4



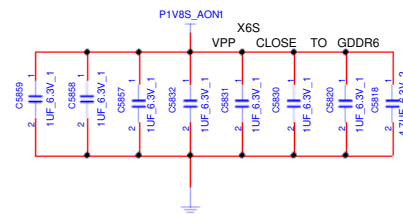
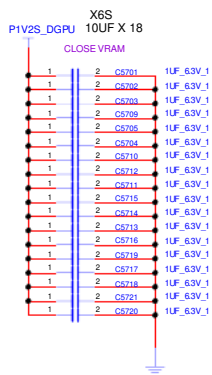






SHARE THE SAME VIA WITH THE VRAM POWER BALL

ENSURE TWO 2GND VIAS AND TWO POWER VIAS FOR EACH CAP



2



# GPU HDMI/DP

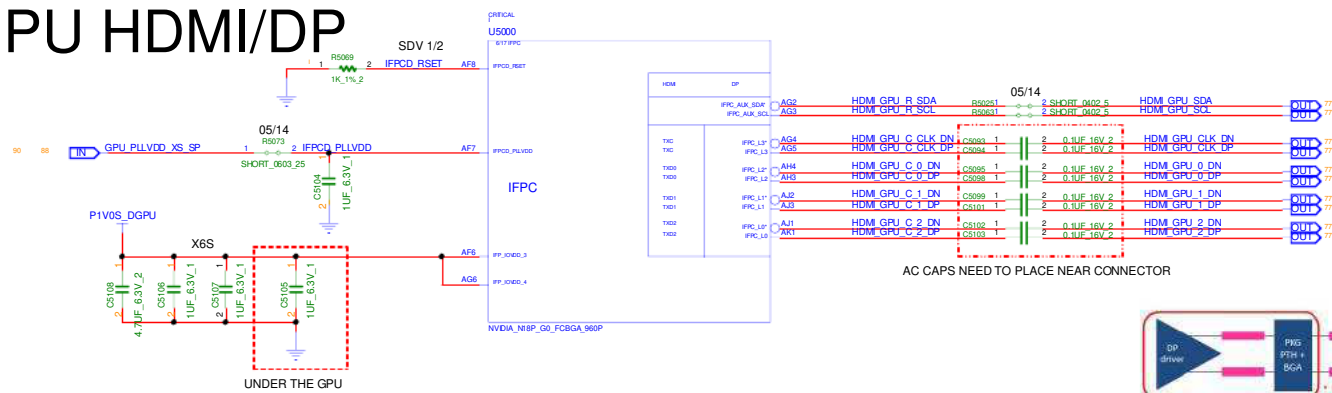
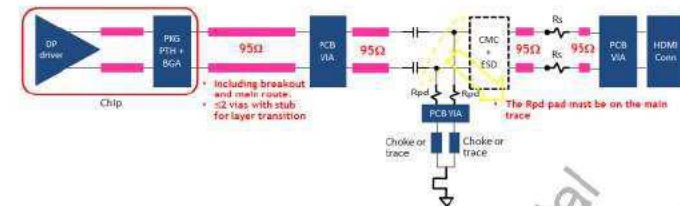


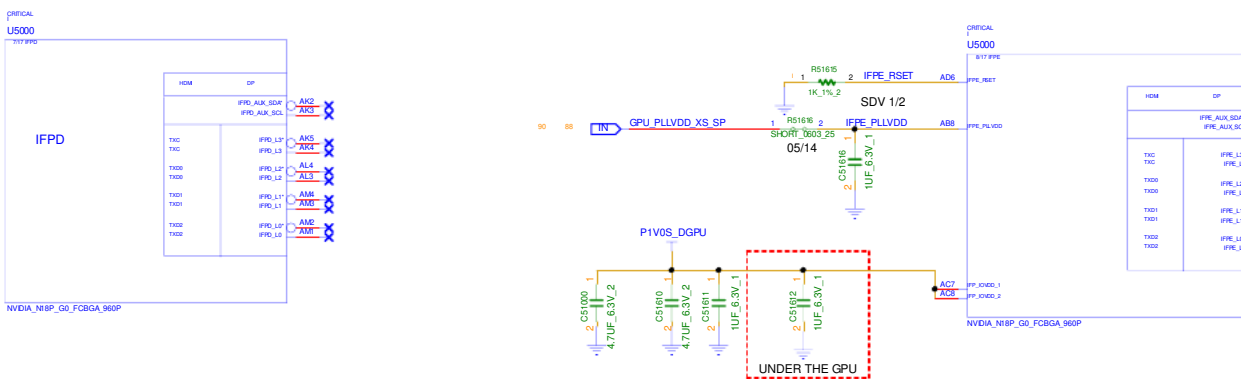
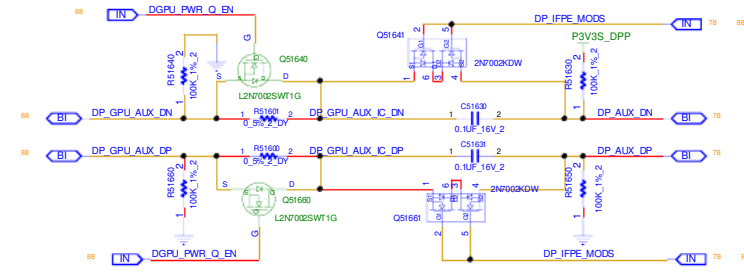
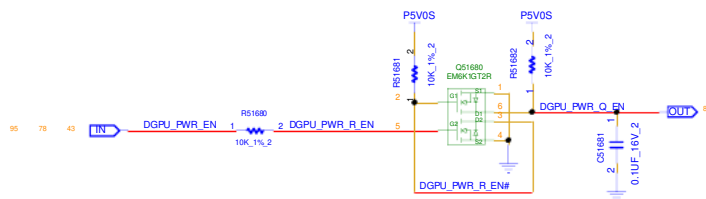
Table 9.3 GB4D-128 Standard Configurations

Link	Standard Display Configurations	
Link A	DisplayPort, DVI (Single Link)	DVI (Dual Link)
Link B	DisplayPort, DVI (Single Link)	
Link C	DisplayPort, <b>HDMI</b> , DVI (Single Link)	
Link D	eDP only (does not support drive of an external display)	
Link E	DisplayPort, HDMI, DVI (Single Link)	

**Note:** Maximum of four independent simultaneously served display heads supported.  
**Note:** eDP is supported on IFPD only



**Figure 9.9 GPU-to-HDMI Connection Diagram**



AC Coupling Capacitor

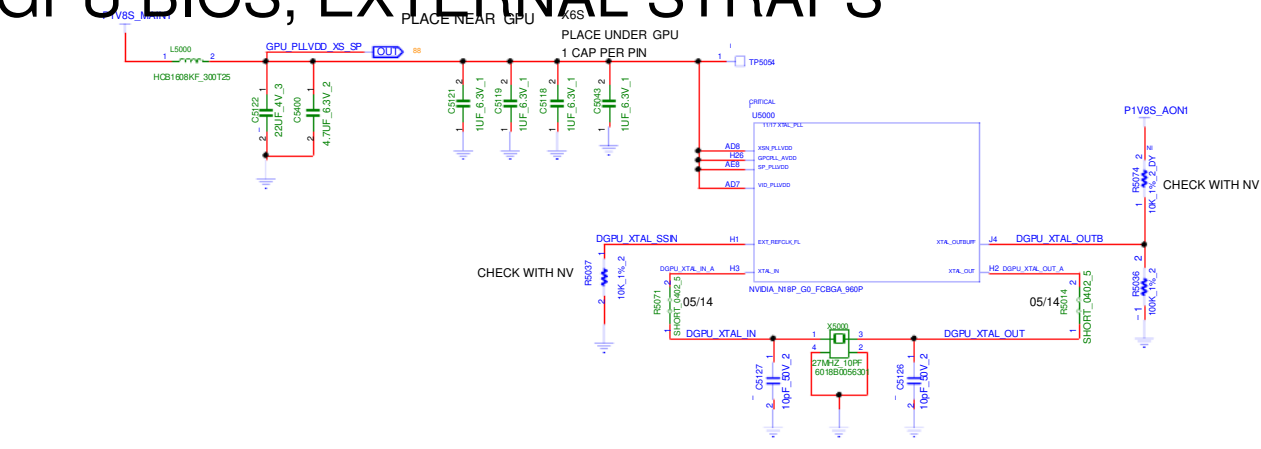
0.1 $\mu$ F 0402, X5R or better, GND voiding below AC coupling cap is required.	Place v connec + surro
---	------------------------------

	Place within 12.5mm of connector. Void size = pad size + surrounding ring of width equal to 1x dielectric height.
--	---

## INVENTEC



# GPU BIOS, EXTERNAL STRAPS



Strap Pins see Note 1			FS_OVERT* Function
ROM_SO see Note 2	ROM_SI	ROM_SCLK	
L	L	L	FS_OVERT* function ENABLED
L	L	H	FS_OVERT* function DISABLED (Reserved; do not configure)
all other configurations			(Invalid; do not configure)

Table 4. N18P-G62/G61 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade
8 Gb	2Chx256Mx16	1.2V	Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps
			Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps

Table 5.3 RAMCFG

Strap Pins see Note			RAMCFG Setting Number (see Memory RVL for memory configs corresponding to these numbers)
STRAP2	STRAP1	STRAP0	
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

Strap Pins See Note			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0

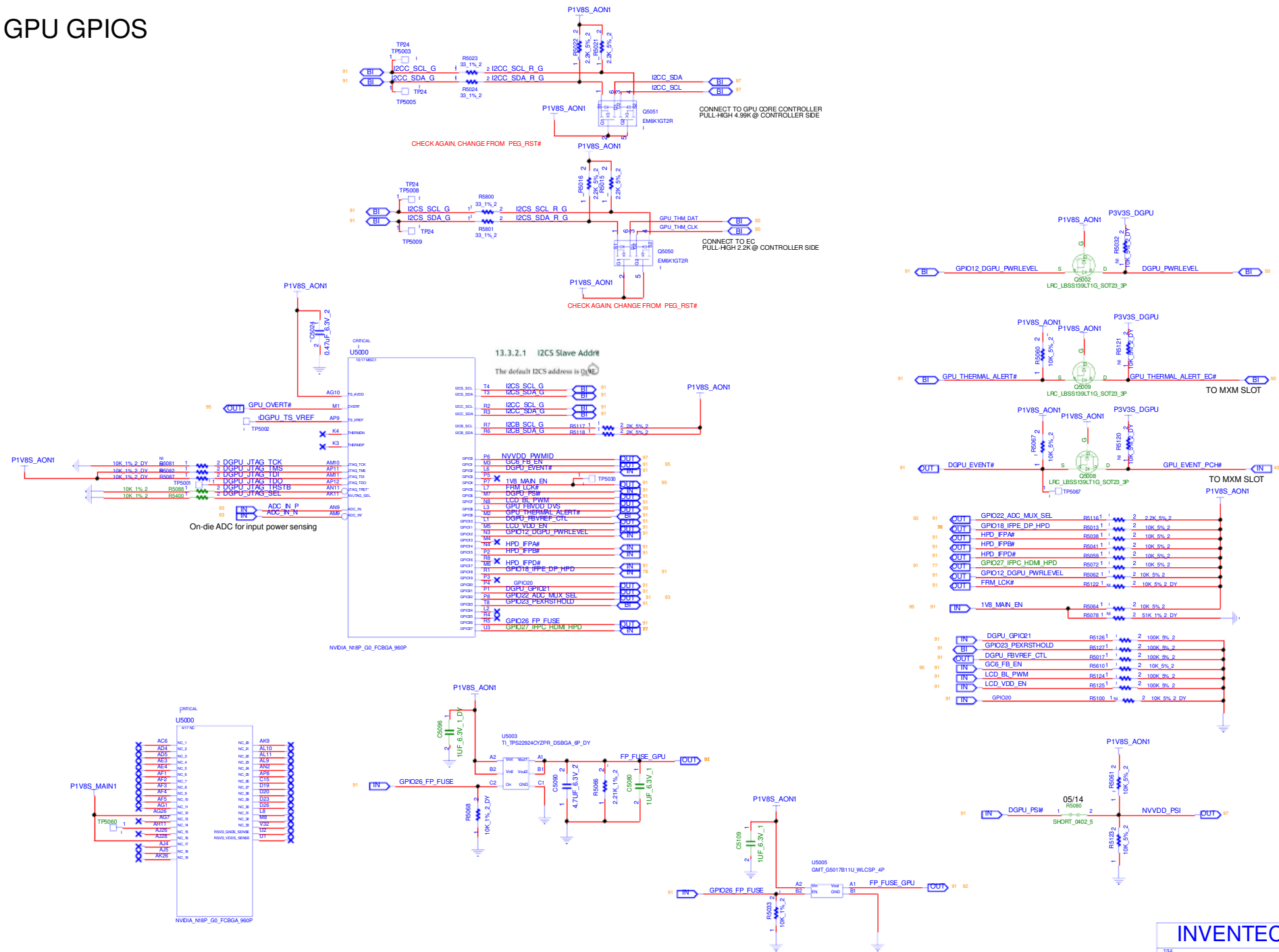
DEFAULT: MICRON

ALL R VALUE IS 100K

VENDER	DENSITY	VENDER PN	IEC PN	STRAP	R5002	R5048	R5009	R5050	R5011	R5051
MICRON	2CHx256Mx16	MT61K256M32JE-14:A	6019B1983601	0X1	6013A0014701	NI	NI	6013A0014701	NI	6013A0014701

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## GPU GPIOs



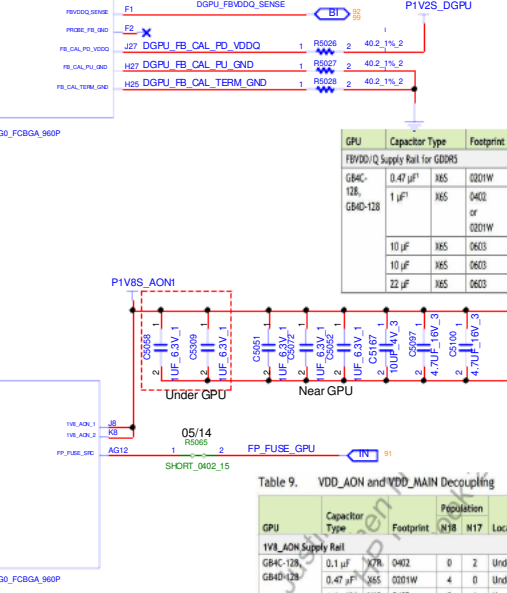
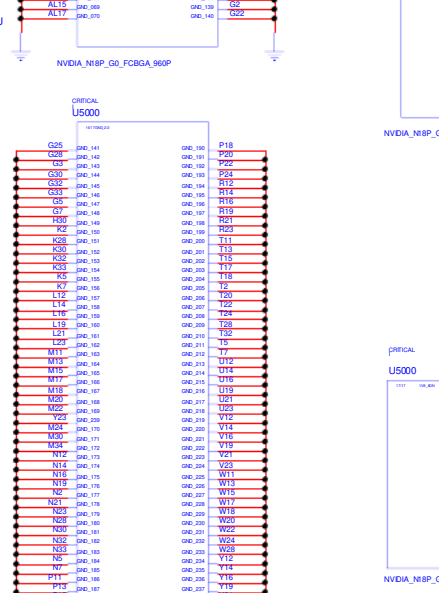
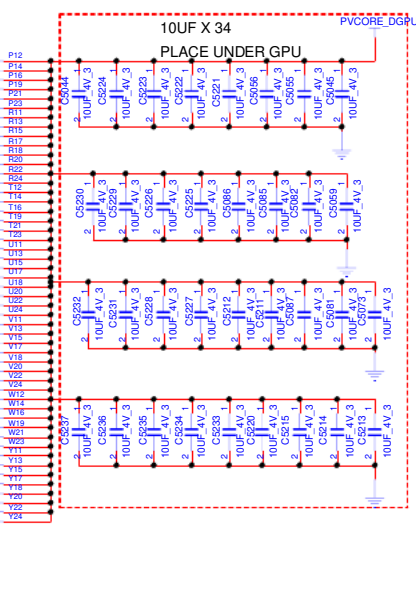
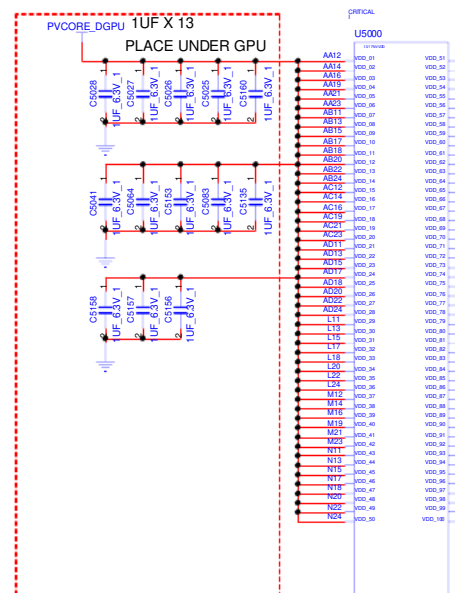
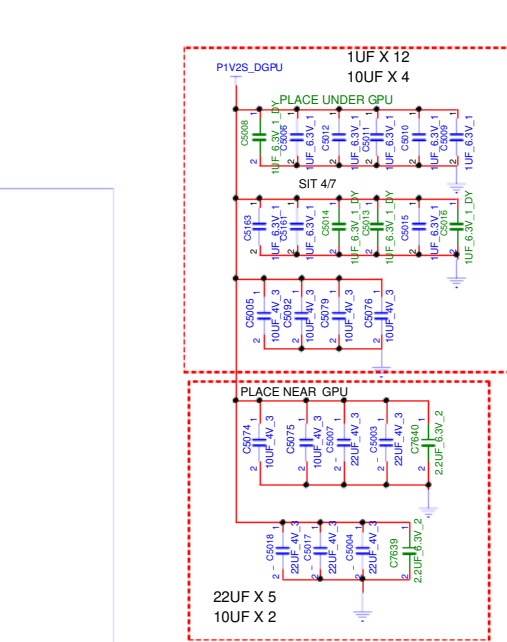
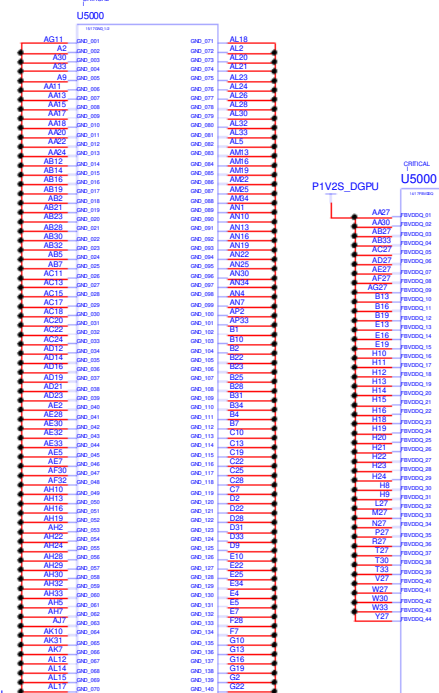
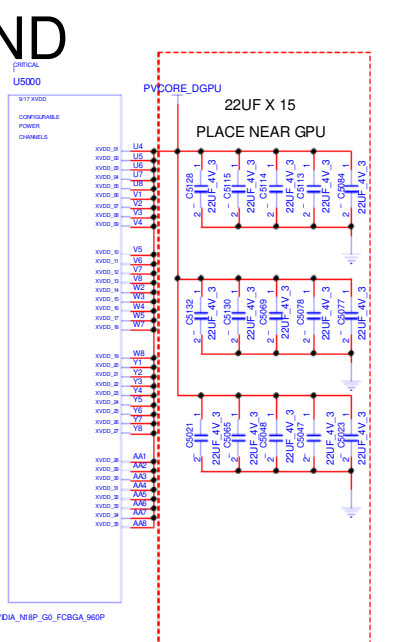
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PCB P/N	60XXXXXXXXXX	PCB VER	XXXX								
				SHEET		91	of	101			

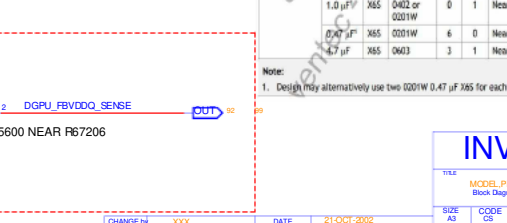
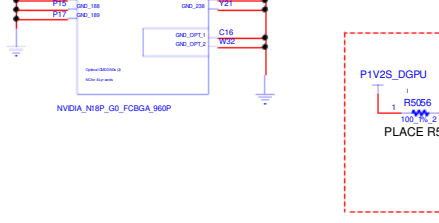
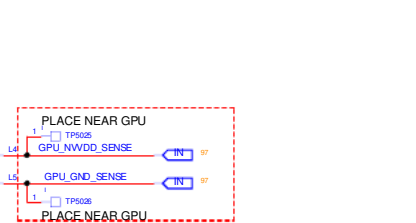


GPU	Capacitor Type	Footprint	Population		Location
			N18	N17	
<b>NVVDD Supply Net</b>					
GB4C-128, GB4D-128	10 $\mu$ F	X6S 0603	34	21	Under GPU
	0.47 $\mu$ F <sup>1</sup>	X6S 0402 or 0201W	0	13	Under GPU
	10 $\mu$ F	X6S 0603	0	11	Near GPU
	22 $\mu$ F	X6S 0805	15	10	Near GPU
	4.7 $\mu$ F	X6S 0603	0	2	Near GPU
	330 $\mu$ F	POS 7343	0	1	Near GPU

GPU	Capacitor Type	Footprint	Population		Location
			N18	N17	
<b>NVVDD Supply Net</b>					
GB4C-128, GB4D-128	10 $\mu$ F	X6S 0603	34	21	Under GPU
	0.47 $\mu$ F <sup>1</sup>	X6S 0402 or 0201W	0	13	Under GPU
	10 $\mu$ F	X6S 0603	0	11	Near GPU
	22 $\mu$ F	X6S 0805	15	10	Near GPU
	4.7 $\mu$ F	X6S 0603	0	2	Near GPU
	330 $\mu$ F	POS 7343	0	1	Near GPU



GPU	Capacitor Type	Footprint	N18	N17	Location
FBVDD/Q Supply Rail for GDRs					
GBAC-128	0.47 $\mu$ F	X6S 0201W	24	0	Under GPU
GBAD-128	1 $\mu$ F	X6S 0402 or 0201W	0	12	Under GPU
	10 $\mu$ F	X6S 0603	4	4	Under GPU
	10 $\mu$ F	X6S 0603	2	2	Near GPU
	22 $\mu$ F	X6S 0603	5	5	Near GPU

Table 9. VDD\_AON and VDD\_MAIN Decoupling

GPU	Capacitor Type	Footprint	Population		
			N18	N17	Location
1V1A0N Supply Rail					
GB42-128	0.1 $\mu$ F	0078	0	2	Under GPU
GB42-128	0.47 $\mu$ F	0051	4	0	Under GPU
	1.0 $\mu$ F	0052 or 0201W	0	1	Near GPU
	0.07 $\mu$ F	0051	6	0	Near GPU
	4.7 $\mu$ F	0063	3	1	Near GPU

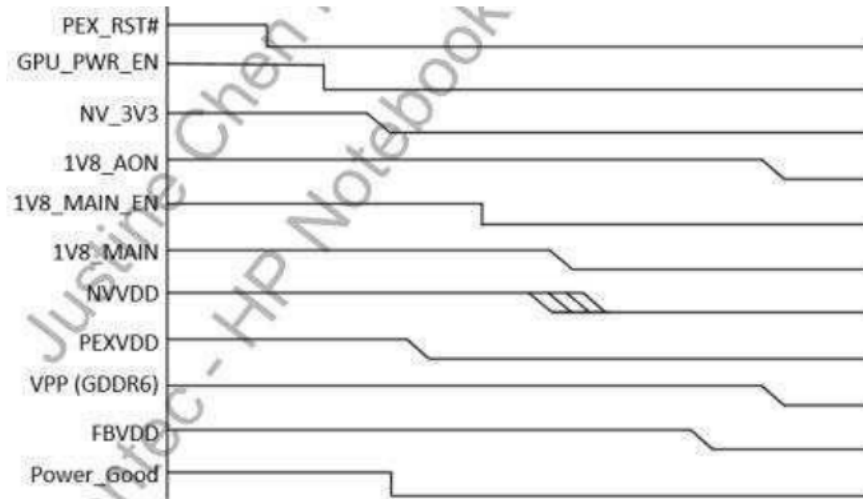
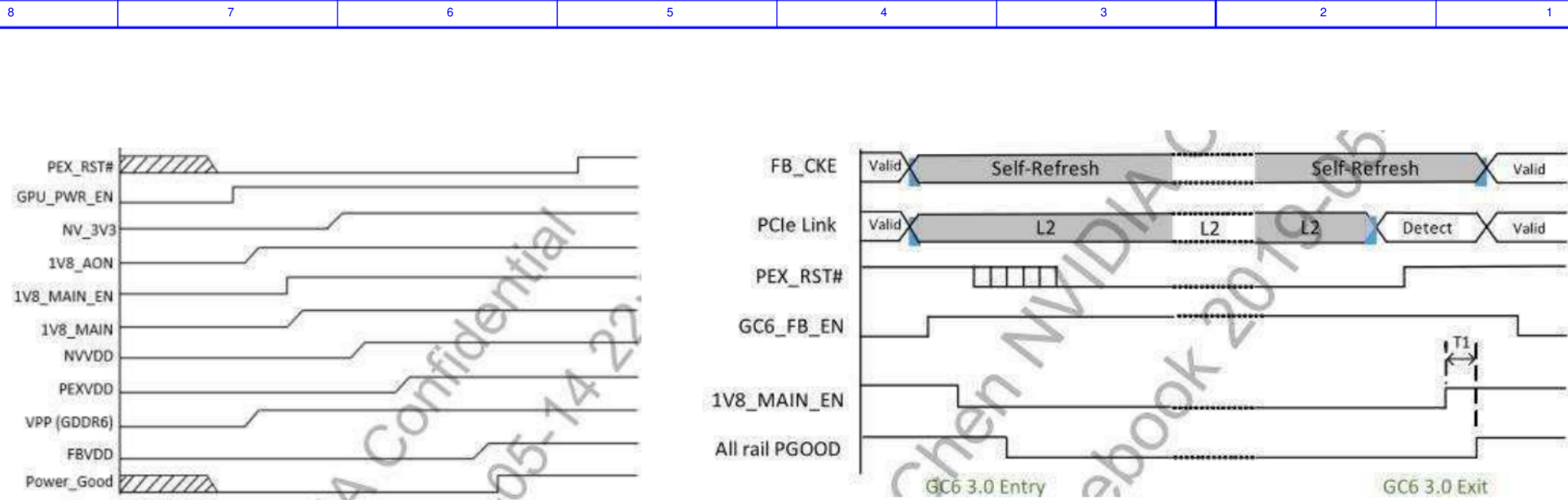
Note:

- Design may alternatively use two 0201W 0.47  $\mu$ F X65 for each 0201W 1  $\mu$ F.

1. Design may alternatively use two Q201W 0.47  $\mu$ F X6S for each Q201W 1  $\mu$ F.





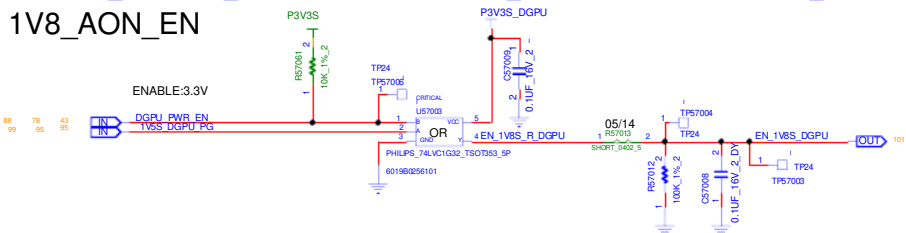
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Block Diagram

SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
SHEET 94 of 101			

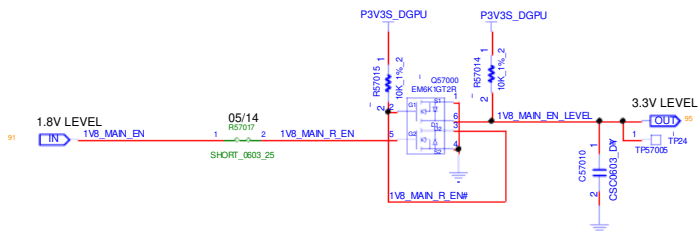
CHANGE by PCB P/N	XXX 60xxxxxxxx	DATE PCB VER	21-OCT-2002 XXX
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POWER\_ON:P1V8S\_AON1-->P1V8S\_MAIN1-->NVVDD-->PEX\_VDD-->FBVDD  
POWER\_OFF:PEX\_VDD-->NVVDD-->P1V8S\_MAIN1-->FBVDD-->P1V8S\_AON1

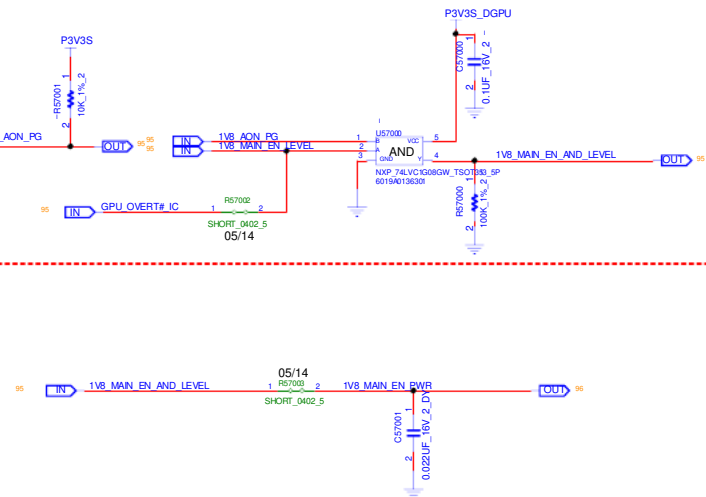
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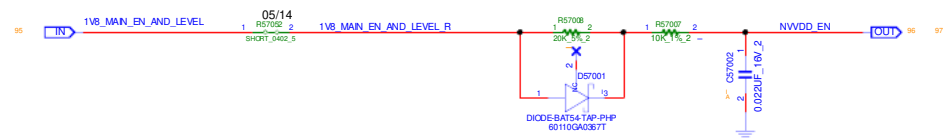
## 1V8\_MAIN\_EN LEVEL SHIFT



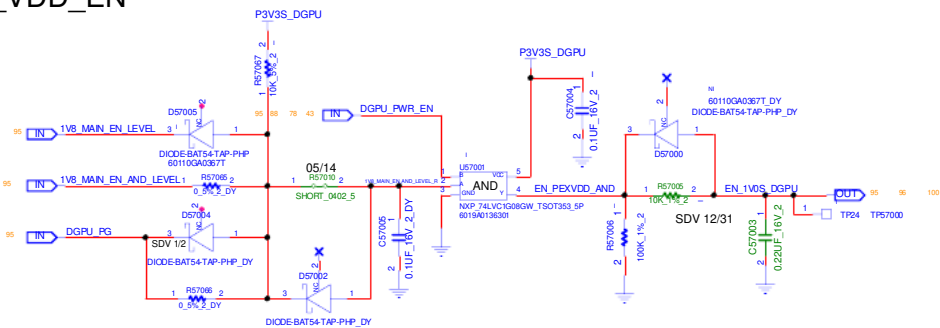
## 1V8\_MAIN\_EN



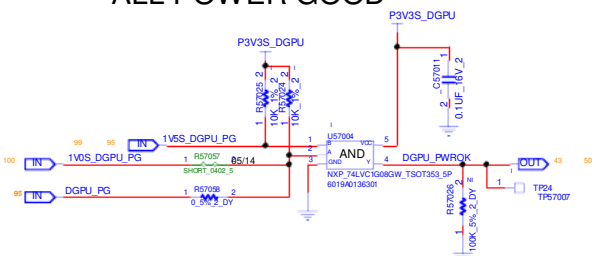
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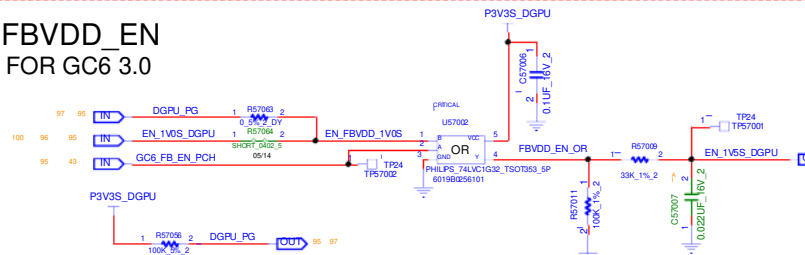
## PEX\_VDD\_EN



## ALL POWER GOOD



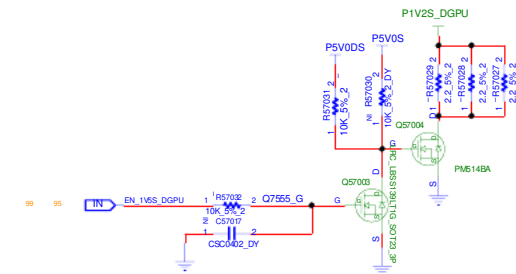
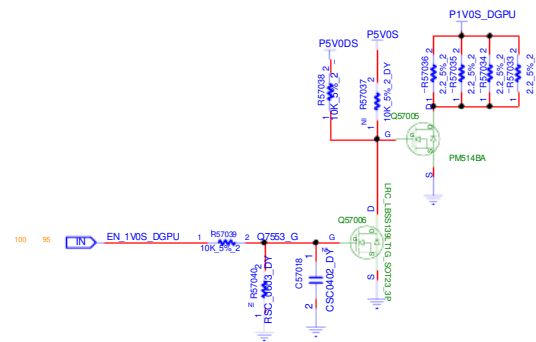
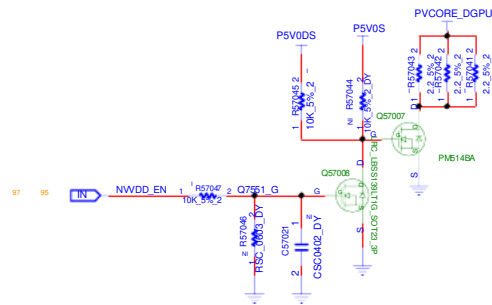
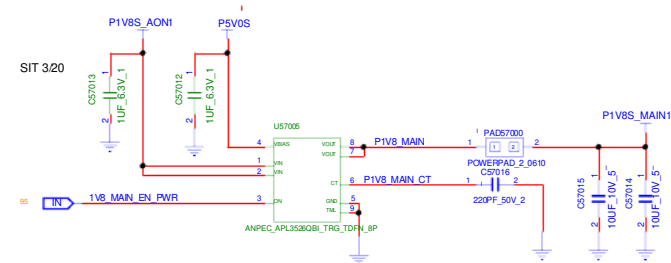
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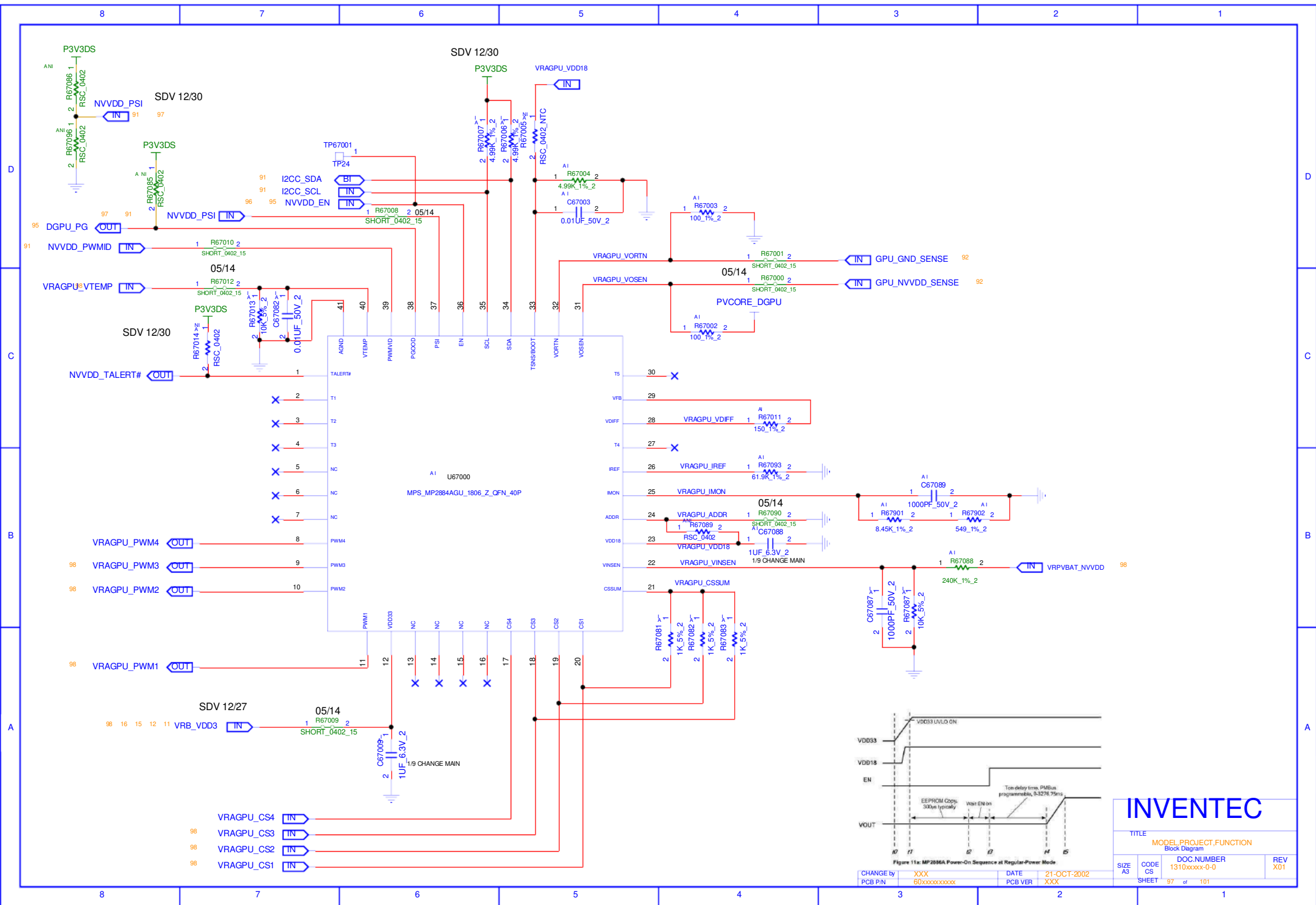


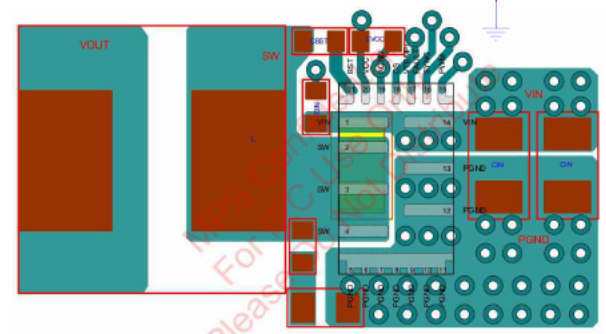
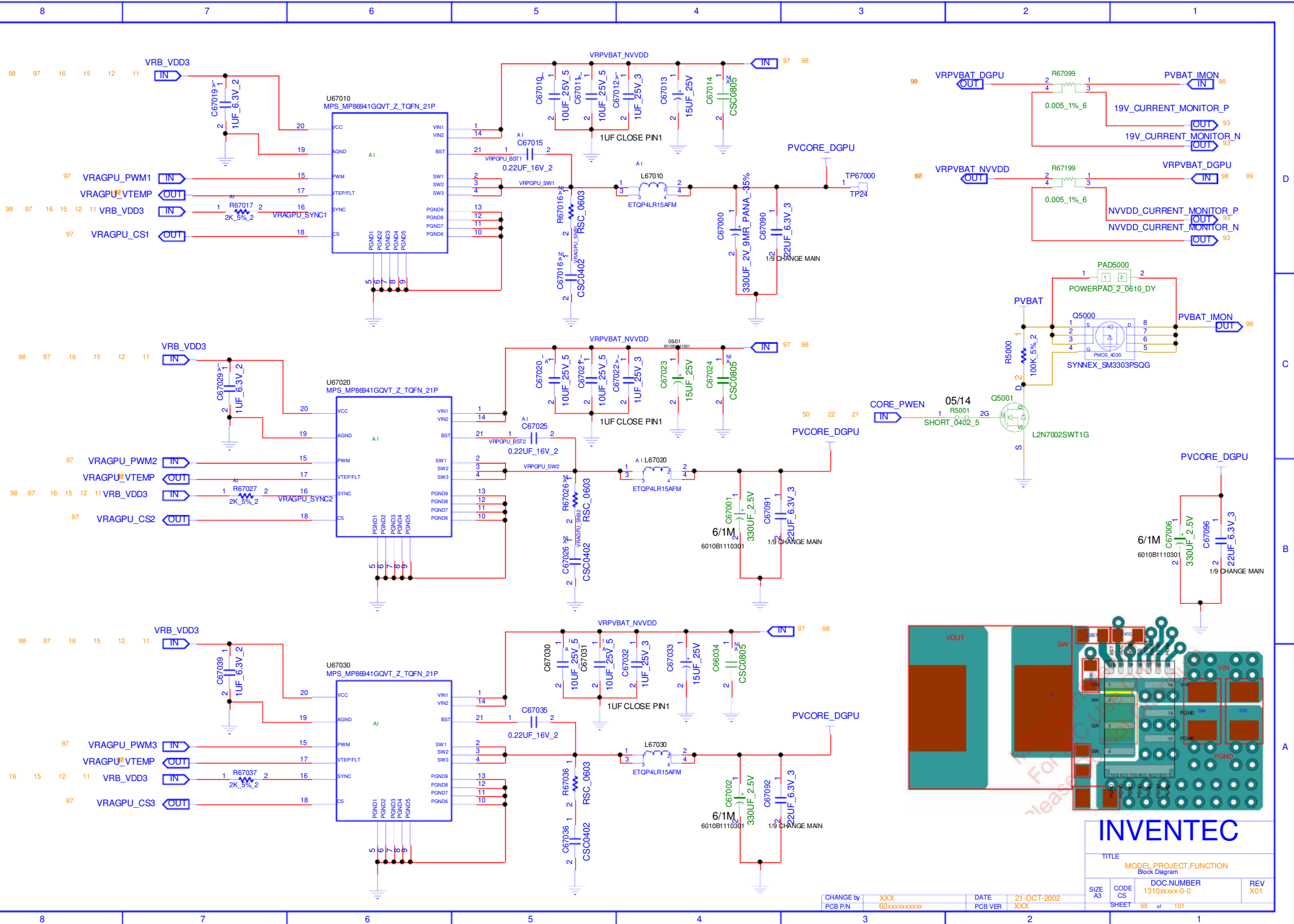
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SHEET	66	of 101	

CHANGE IN PCB PIN XXXXXXXXXXXX DATE 21-OCT-2002 PCB VER XXX

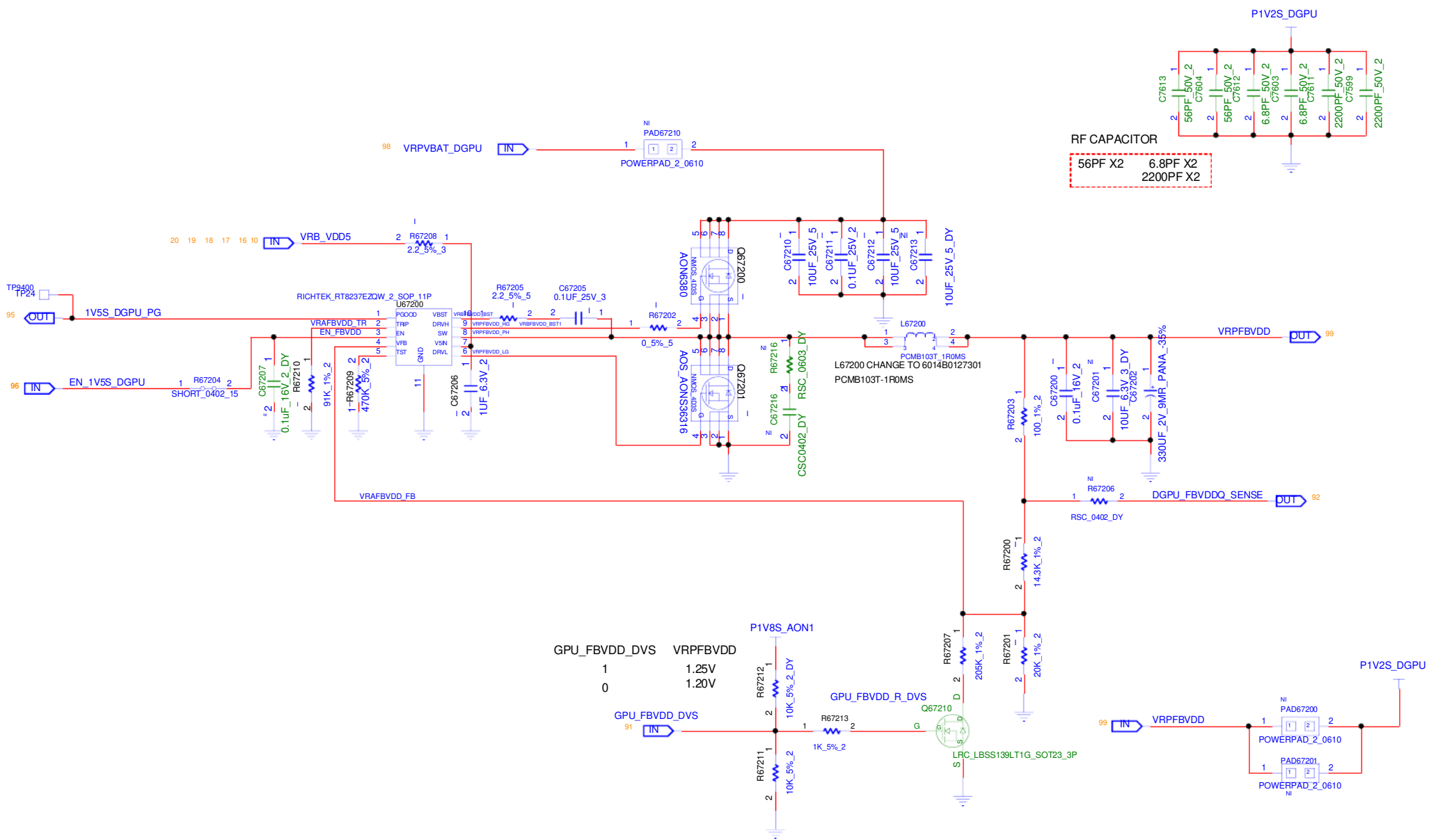






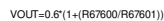
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SHEET		98 of 101	



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SHEET		99		of		101					



CHANGE by	XXX	DATE	21-OCT-2002	SIZE	A3	CODE	CS	1310xxxxx-0-0	X01
PCB P/N	60xxxxxxxxxx	PCB VER	XXX			SHEET	100	of 101	





SIZE A3	CODE CS	DOC. NUMBER 1310xxxx-0-0	REV X01
SHEET		101 of 101	